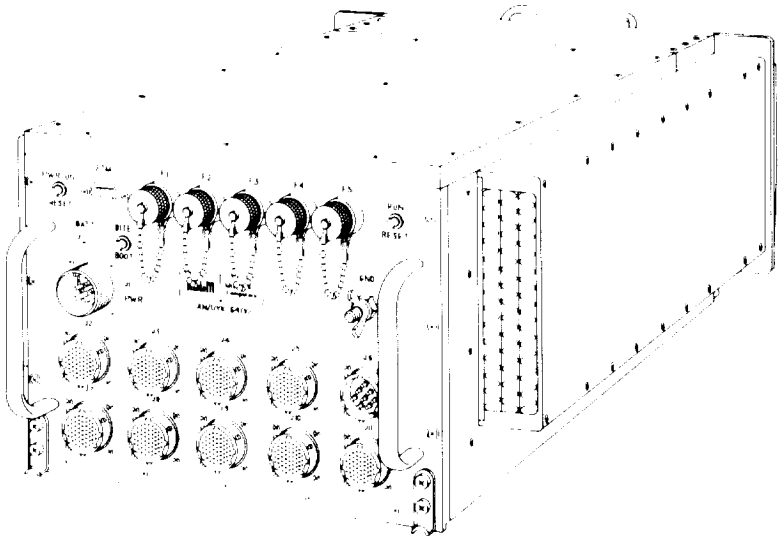
DIRECT SUPPORT AND GENERAL SUPPORT MAINTENANCE MANUAL FOR DATA PROCESSING SET AN/UYK-64(V)

AN/UYK-64(V)1	(NSN 7035-01-155-0153)
AN/UYK-64(V)1x	(NSN 7035-01-155-0154)
AN/UYK-64(V)2	(NSN 7035-01-166-7855)
AN/UYK-64(V)2x	(NSN 7035-01-155-0155)
AN/UYK-64(V)3	(NSN 7035-01-155-0156)
AN/UYK-64(V)3x	(NSN 7035-01-155-0157)
AN/UYK-64(V)4	(NSN 7035-01-155-0158)
AN/UYK-64(V)4x	(NSN 7035-01-155-0159)



HEADQUARTERS, DEPARTMENT OF THE ARMY
13 SEPTEMBER 1985

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5 SAFETY STEPS TO FOLLOW IF SOMEONE IS THE VICTIM OF ELECTRICAL SHOCK

1. DO NOT TRY TO PULL OR GRAB THE INDIVIDUAL

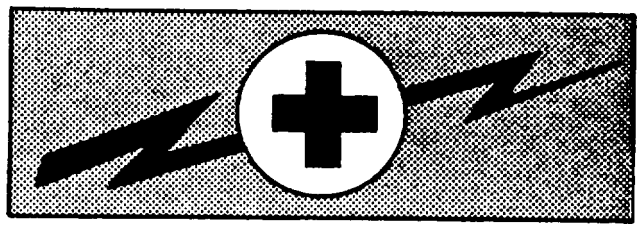
2. IF POSSIBLE, TURN OFF THE ELECTRICAL POWER

3. IF YOU CANNOT TURN OFF THE ELECTRICAL POWER, PULL, PUSH, OR LIFT THE PERSON TO SAFETY USING A WOODEN POLE OR A ROPE OR SOME OTHER INSULATING MATERIAL

4. SEND FOR HELP AS SOON AS POSSIBLE

5. AFTER THE INJURED PERSON IS FREE OF CONTACT WITH THE SOURCE OF ELECTRICAL SHOCK, MOVE THE PERSON A SHORT DISTANCE AWAY AND IMMEDIATELY START ARTIFICIAL RESUSCITATION

WARNING



HIGH VOLTAGE

is used in the operation of this equipment

DEATH ON CONTACT

may result if personnel fail to observe safety precautions

Never work on electronic equipment unless there is another person nearby who is familiar with the operation and hazards of the equipment and who is competent in administering first aid. When the technician is aided by operators, he must warn them about dangerous areas.

Whenever possible, the power supply to the equipment must be shut off before beginning work on the equipment. Take particular care to ground every capacitor likely to hold a dangerous potential. When working inside the equipment, after the power has been turned off, always ground every part before touching it.

Be careful not to contact high-voltage connections or 115 volt ac input connections when installing or operating this equipment.

Whenever the nature of the operation permits, keep one hand away from the equipment to reduce the hazard of current flowing through the body.

Warning: Do not be misled by the term “low voltage.” Potentials as low as 50 volts may cause death under adverse conditions.

For Artifical Respiration, refer to FM 21-11

WARNING

FLAMMABLE LIQUIDS

are used in cleaning the equipment. Keep them away from heat and open flames.

Technical Manual

No. 11-7021-202-34

HEADQUARTERS
DEPARTMENT OF THE ARMY
Washington, DC, 13 September 1985

Direct Support and General Support Maintenance Manual for AN/UYK-64(V) DATA PROCESSING SET

AN/UYK-64(V)1 (NSN 7035-01-155-0153)
AN/UYK-64(V)1x (NSN 7035-01-155-0154)
AN/UYK-64(V)2 (NSN 7035-01-166-7855)
ANWYK-64(V)2x (NSN 7035-01-155-0155)
AN/UYK-64(V)3 (NSN 7035-01-155-0156)
AN/UYK-64(V)3x (NSN 7035-01-155-0157)
AN/UYK-64(V)4 (NSN 7035-01-155-0158)
AN/UYK-64(V)4x (NSN 7035-01-155-0159)

REPORTING ERRORS AND RECOMMENDING IMPROVEMENTS

You can help improve this manual. If you find any mistakes or if you know of a way to improve the procedures, please let us know. Mail your letter, DA Form 2028 (Recommended Changes to Publications and Blank Forms), or DA Form 2028-2 located in the back of this manual direct to: Commander, US Army Communications-Electronic Command and Fort Monmouth, ATTN: AMSEL-ME-MP, Fort Monmouth, New Jersey 07703-5007. In either case, a reply will be furnished direct to you.

LIST OF ILLUSTRATIONS

LIST OF TABLES

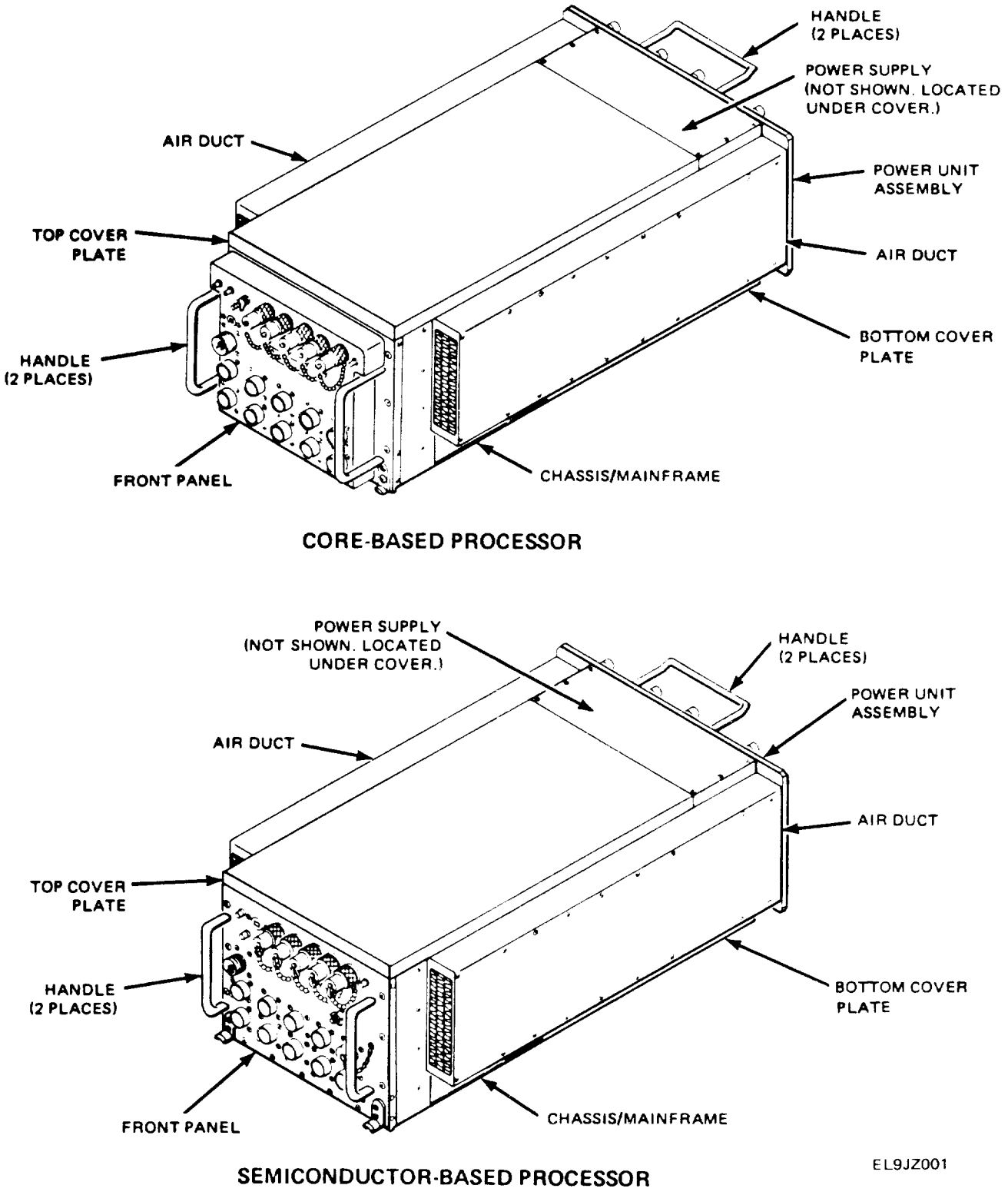


Figure 1. Data Processing Set, AN/UYK-64(V), Typical

CHAPTER 1

INTRODUCTION

Section 1. GENERAL INFORMATION

1-1. SCOPE

This manual contains Direct Support/General Support Maintenance information for the Data Processing Set AN/UYK-64(V) (figure 1), Appendices to this manual provide a glossary, index, list of references, configuration data, and other items of information applicable to the maintenance of the Data Processing Set AN/UYK-64(V). Except as otherwise noted, references to processor apply to all eight configurations (versions) of the Data Processing Set AN/UYK-64(V); i.e., (V)1, (V)1 X, (V)2, (V)2X, (V)3, (V)3X, (V)4, and (V)4X.

This chapter contains data relating to forms, records, and reports, and it provides general information that familiarizes the reader with the equipment. Equipment characteristics, capabilities, features, major component descriptions, and a discussion of equipment operating principles are included. Equipment interface information and instructions concerning safety, care, and handling of the equipment are also provided.

1-2. CONSOLIDATED INDEX OF ARMY PUBLICATIONS AND BLANK FORMS

Refer to the latest issue of DA Pam 310-1 to determine if there are new editions, changes, or additional publications pertaining to the Data Processing Set AN/UYK-64(V).

1-3. MAINTENANCE FORMS, RECORDS, AND REPORTS

a. **Reports of Maintenance and Unsatisfactory Equipment.** Department of the Army forms and procedures used for equipment maintenance will be those prescribed by DA Pam 738-750 as contained in Maintenance Management Update.

b. **Reports of Packaging and Handling Deficiencies.** Fill out and forward SF 364 (Report of Discrepancy (ROD)), as prescribed in AR 735-11-2/DLAR 4140.55/NAVMATINST 4355.73A/AFR 400-54/MCO 4430.3F.

c. **Discrepancy in Shipment Report (DISREP) SF 361).** Fill out and forward Discrepancy in Shipment Report (DISREP), (SF 361), as prescribed in AR 55-38/NAVSUPINST 4610.33C/ AFR 75-18/MCO P4610.19D/DLAR 4500.15.

1-4. ADMINISTRATIVE STORAGE

Equipment issued to and used by Army activities will have preventive maintenance performed in accordance with the preventive maintenance checks and service (PMCS) charts in TM 11-7021-202-12 before being placed in administrative storage, When removing the equipment from administrative storage, the PMCSs should be performed to assure operational readiness. Disassembly and repacking of equipment for shipment or limited storage are covered in chapter 5.

1-5. DESTRUCTION OF ARMY ELECTRONICS MATERIAL

Destruction of Army electronics materiel to prevent enemy use shall be accomplished in accordance with TM 750-244-2.

1-6. REPORTING EQUIPMENT IMPROVEMENT RECOMMENDATIONS (EIRs)

If the Data Processing Set AN/UYK-64(V) needs improvement, let us know. Send us an EIR. You, the user, are the only one who can tell us what you don't like about the processor. Let us know why you don't like the design. Put it on an SF 368 (Quality Deficiency Report). Mail it to: Commander, US Army Communications-Electronics Command and Fort Monmouth, ATTN: AMSEL-PA-MA-D, Fort Monmouth, New Jersey 07703-5023. We'll send you a reply.

1-7. OFFICIAL NOMENCLATURE, NAMES, AND DESIGNATORS

Table 1-1 provides a list of the processor major assemblies and subassemblies. The list identifies each item by its common name, official nomenclature, and equipment designator (if applicable).

Table 1-1. Nomenclature Cross-Reference List, Data Processing Set AN/UYK-64(V)

Common Name	Official Nomenclature
Processor	Data Processing Set AN/UYK-64(V) (Versions V1, V1X, V2, V2X, V3, V3X, V4, V4X)
Chassis/Mainframe	Processor Chassis Assembly (A25)
Motherboard	Motherboard Assembly (P/N 109883 or P/N 110800)
Core Memory	Model 201964 kB Core Memory (A16 through A22)
Semi Memory	Model 2030512 kB Semiconductor Memory (A16 through A22)
FPU	Model 1751 FPU Card Set, (A13 through A15) (P/N 110966-01 or -02)
CPU	Models 5711 or 5710 CPU Card Set (A9 through A12) (P/N 110972-02 or P/N 110973-01)
I/O	I/O Card Set (A1 through A8)
A1, I/O PCB	(I/O cards (A1 through A8) are configuration-dependent, as defined in appendices C, D, and E.)
A2, I/O PCB	
A3, I/O PCB	
A4, I/O PCB	
A5, I/O PCB	
A6, I/O PCB	
A7, I/O PCB	
A8, I/O PCB	
A9, CPU PFP PCB	Models 5710 or 5711 CPU PFP PCB (P/N 109828-01)
A10, CPU Data PCB	Models 5710 or 5711 CPU Data PCB (P/N 109824-01)

Table 1-1. Nomenclature Cross-Reference List, Data Processing Set AN/UYK-64(V) — Continued

Common Name	Official Nomenclature
A11, CPU PROM PCB	Models 5710 or 5711 CPU PROM PCB (P/N 109836-02) or (P/N 109836-04)
A12, CPU MAP PCB	Models 5710 or 5711 (P/N 109832-01)
A13, FPU-A PCB	Model 1751 FPU-A PCB (P/N 109856-01)
A14, FPU-B PCB	Model 1751 FPU-B PCB (P/N 109860-01)
A15, FPU-CE PCB	Model 1751 FPU-CE PCB (P/N 110941-01)
A15, FPU-C66 PCB	Model 1751 FPU-C66 PCB (P/N 110984-01)
A16, lMC/RMC PCB	Model 1755 lMC/RMC PCB (P/N 109848-01)
A16, SC MEM ERCC PCB	Model 1754 SC MEM ERCC PCB (P/N 109852-01)
A17, Y-Driver PCB	Model 2019 Y-Driver PCB (P/N 107825-01)
A17, SC MEM CTRL PCB	Model 1753 SC MEM CTRL PCB (P/N 109844-01)
A18, X-Driver PCB	Model 2019 X-Driver PCB (P/N 107825-02)
A18, SC 128 kB Array PCB	Model 2030 SC 128 kB Array PCB (P/N 109840-01)
A19, 32 kB Word Stack PCB	Model 201932 kB Word Stack PCB (P/N 105963-01)
A19, SC 128 kB Array PCB	Model 2030 SC 128 kB Array PCB (P/N 109840-01)
A20, Y-Driver PCB	Model 2019 Y-Driver PCB (P/N 107825-01)
A20, SC MEN CTRL PCB	Model 1753 SC MEM CTRL PCB (P/N 109844-01)
A21, X-Driver PCB	Model 2019 X-Driver PCB (P/N 107825-02)
A21, SC 128 kB Array PCB	Model 2030 SC 128 kB Array PCB (P/N 109840-01)
A22, 32 kB Word Stack PCB	Model 201932 kB Word Stack PCB (P/N 105963-01)

Table 1-1. Nomenclature Cross-Reference List, Data Processing Set AN/UYK-64(V) — Continued

Common Name	Official Nomenclature
A22, SC 128 kB Array	Model 2030 SC 128 kB Array PCB (P/N 109840-01)
A23, Power Supply	Model 5617 AC Power Supply (P/N 110684-01) or Model 5687 DC Power Supply (P/N 112676-01)
A24, EMI Filter	Model 3883 AC EMI Filter (P/N 112241-01) or Model 3884 DC EMI Filter (P/N 113081-01)

Section II. EQUIPMENT DESCRIPTION DATA

1-8. EQUIPMENT DESCRIPTION

The processor is one in a family of military computers supporting scientific and real-time applications requiring high speed processing and throughput. The processor provides proven reliability and high resistance to severe operating environments.

The processor is packaged in a single, conductively cooled air-transport rack (ATR) chassis/mainframe with wraparound heat exchanging. The chassis/mainframe provides an exit path for heat being generated by the power supply and printed-circuit boards (PCBs). Cool air sucked in at the front of the processor is drawn through the air ducts on each side of the chassis absorbing heat as the air flows over the heat-conducting surfaces. The heated air is exhausted at the rear of the unit. Access for servicing the processor is facilitated by the removal of the power supply, front panel, and top and bottom cover plates,

Depending upon processor configuration (table 1-1), there may be either core or semiconductor memory configured with one of two types of central processing unit (CPU) PROM printed circuit boards (PCBs), one of two types of floating point unit (FPU) “C” PCBs; and one of two types of motherboard. Processor may be powered by an ac or dc power supply. Additionally, a wide selection of input/output (I/O) interface PCBs may be employed (Appx C, D and E).

Eight input/output (I/O) slots are provided in the processor’s card cage for a maximum configuration of eight I/O interfaces. The I/O interfaces contain the interface logic and circuits that effect the two-way transfer of information and data between the processor’s CPU section and peripheral devices. It includes direct memory access for high-speed devices.

A built-in test (BITE) feature provides a series of self-test diagnostics that are automatically performed at power-up as an aid in assuring processor readiness and the isolation of fault conditions.

A battery back up feature for semiconductor memory configurations can be implemented to retain memory integrity in the event of power interruption.

Operator control of the CPU is provided through a system terminal when the CPU is in the virtual console (VC) mode. This mode permits boot/load operations, program loading, and diagnostic program loading. In addition, it provides the operator with the means of inserting break points, examining and/or modifying the contents of a memory location or an internal software register, injecting standard program control functions, and the running of diagnostics.

1-9. EQUIPMENT CHARACTERISTICS, CAPABILITIES, AND FEATURES

Table 1-2 provides a list of the processor’s characteristics, capabilities, and features.

Table 1-2. Processor Characteristics, Capabilities, and Features

Item	Data
CPU	
Architecture:	Microprogrammed
Microinstruction Word Length:	64 bits
Microinstruction Capacity:	4096 Words
Instruction Length:	16 bits (single), 32 bits (double)
Hardware Accumulators:	4 Integer — 16 bits
Index Registers:	2 Integer — 16 bits
Instruction Types:	Fixed-Point Arithmetic Logical Operations Character Operations Floating Point
Addressing Modes:	Direct Immediate Indexed Program Counter Relative Accumulator Relative Multi-Level Indirect
Bus Structure:	Separate Memory In/Out I/O Prefetch Processor
SEMICONDUCTOR MEMORY	
Capacity:	256k Words internal
Cycle Time:	500. nanoseconds
Interleaving:	2-way or 4-way
Module Capacity:	64k Words, 21 bits
Error Checking:	Single bit ERCC (5-bit code)

Table 1-2. Processor Characteristics, Capabilities, and Features — Continued

Item	Data
CORE MEMORY	
Capacity:	64k Words internal 960k Words external
Cycle Time:	1.0 microsecond internal 1.1 microsecond external
Module Capacity:	32k Words, 17-bits
Error Checking:	Single bit, odd parity
INPUT/OUTPUT (I/O)	
I/O Types:	Programmed Data Channel
Interrupts:	16 Priority Interrupt Levels
Addressable Devices:	59
DIMENSIONS/WEIGHT	
Chassis:	7.62 in. x 13.30 in. x 24.19 in. (19.35 cm x 33.78 cm x 61.44 cm); 90 lb (40.90 kg).
ENVIRONMENT	
Units of the Processor (system terminal excepted) are designed to the following environmental specifications, which meet or exceed those of MIL-E-5400 and MIL-E-16400.	
Inlet Air Temperature:	Standard: 0.0°C to + 50°C (+32°F to +105°F) Wide: -25°C to +60°C (+19°F to +140°F) Extreme: -55°C to +71°C (+41°F to +159°F) (Core Memory only) (MIL-E-5400, Class 2, MIL-E-16400, Range 1)

Table 1-2. Processor Characteristics, Capabilities, and Features — Continued

Item	Data
Humidity:	95% relative
Vibration:	
With vibration isolators:	10g, 5-200 Hz (MIL -E-5400, Curve IVa)
Hardmounted:	2g, 5-2000 Hz (MIL-E-5400, Curve IIa)
Shock:	
With vibration isolators:	400 + lb impact (MIL-E-16400 and MIL-S-901C)
Hardmounted:	15g, 11 ms (MIL-E-400)
Altitude:	80,000 ft (MIL-E-5400, Class 2)
EMI Characteristics:	MIL-STD-461A
Explosive atmosphere, sand and dust, salt fog, and fungus resistant in accordance with MIL-E-5400 and MIL-E-16400.	
POWER	
Input Power:	100-130V ac, 47-63 Hz or 400 Hz, single-phase 220V ac (180-240), 47-63 Hz, single-phase 115V ac or 200V ac, 400 Hz, three-phase, MIL-STD-704C 208V ac (180-240), 47-63 Hz, three-phase 28V (24-32)
Power Dissipation:	
555 watts,	Core memory version
575 watts,	Semiconductor memory version
65 watts,	Semiconductor memory during battery back-up (memory only)

1-10. LOCATION AND DESCRIPTION OF MAJOR COMPONENTS

The Processor (all versions) is comprised of the chassis assembly, power supply (ac or dc), power unit assembly (ac or dc), and front panel (part of the Motherboard Assembly). See figure 1-1 and refer to table 1-1. The subparagraphs to follow provide component locations and descriptions.

a. Chassis Assembly. The chassis is comprised of the mainframe, card cage, two air ducts, and the top and bottom cover plates (figures 1-2, 1-3).

b. Motherboard Assembly. The motherboard assembly is located directly below the card cage assembly and printed circuit boards (PCBs). The assembly serves as the prime interface between the electronic components within the processor (e.g., power supply, PCBs, input/output (I/O) connectors, etc.), and the interface between the PCBs and equipment externally connected to the processor. The motherboard is accessed from the bottom of the processor once the bottom cover plate is removed, and from the top of the unit after the top cover plate is removed, and from the top of the unit after the top cover plate and all of the PCBs are removed. See figure 1-3.

c. Power Supply. The 5617 ac power supply or a 5687 dc power supply is housed at the rear of the processor, behind and attached to the power unit assembly. The power supplies are plug-in units. The ac power supply converts external primary 115 V ac power into dc voltages required for processor operation. The dc power supply uses externality supplied 28 V dc to create the dc voltages required for processor operation (fig. 1-1, 1-2, 1-3).

d. EMI Filiter. The 3883 ac EMI filter or 3884 dc EMI filter is located behind the processor's front panel assembly. The filter is employed to eliminate electromagnetic interference (EMI) being generated by the processor power system (fig. 1-4). The EMI filters are plug-in units.

e. Power Unit Assembly. The power unit assembly is mounted at the rear of the processor (fig. 1-2, 1-3) and attaches to the chassis; the power supply is attached to the power unit assembly. The ac version of the power unit assembly is comprised of a cover, power unit (electronics module), and an ac blower fan. The dc version of the unit is comprised of the same components, except the electronics module is not used (fig. 1-6) and a dc blower fan is used.

f. Front Panel Assembly. The front panel of a processor with semiconductor memory (fig. 1-5) contains 11 connectors, a bank of five fuse assemblies, an elapsed time meter (ETM), a PWR ON/RESET indicating pushbutton switch, program 13 UN/RESET indicating pushbutton switch, a BITE/BOOT indicating pushbutton switch, and a grounding lug. A BATT indicator shows whether or not the memory power (+ 5 V) is up.

The front panel of a processor with core memory is similar to the front panel of a processor with semiconductor memory with the following exceptions:

- No **BATT** indicator
- Ground stud moved from right side of the panel to upper left corner of the panel.

. J6 is converted from an 8-pin battery back-up connector to a 55-pin connector for interfacing an external core memory extension chassis.

. Panel is thicker and has a different shape than the panel on the semiconductor version (fig. 1-1).

Up to eight of the 11 connectors on the core memory processor front panel may be used to connect peripheral devices to their respective I/O interface PCBs in slots Al through A8. The remaining three connectors are used for power input (ac or de), connection to a system terminal, and connection to a remote memory. Three of the fuse assemblies on the panels are used when the processor is configured for ac power, and the remaining two are used when the input power is dc. The ETM display indicates accumulated processor running hours. Table 1-3 lists and describes the function of the processor's front panel connectors, indicators, controls, and fuses (fig. 1-5).

1-11. DIFFERENCES BETWEEN MODELS

Table 1-4 provides a matrix depicting the eight versions of the processor.

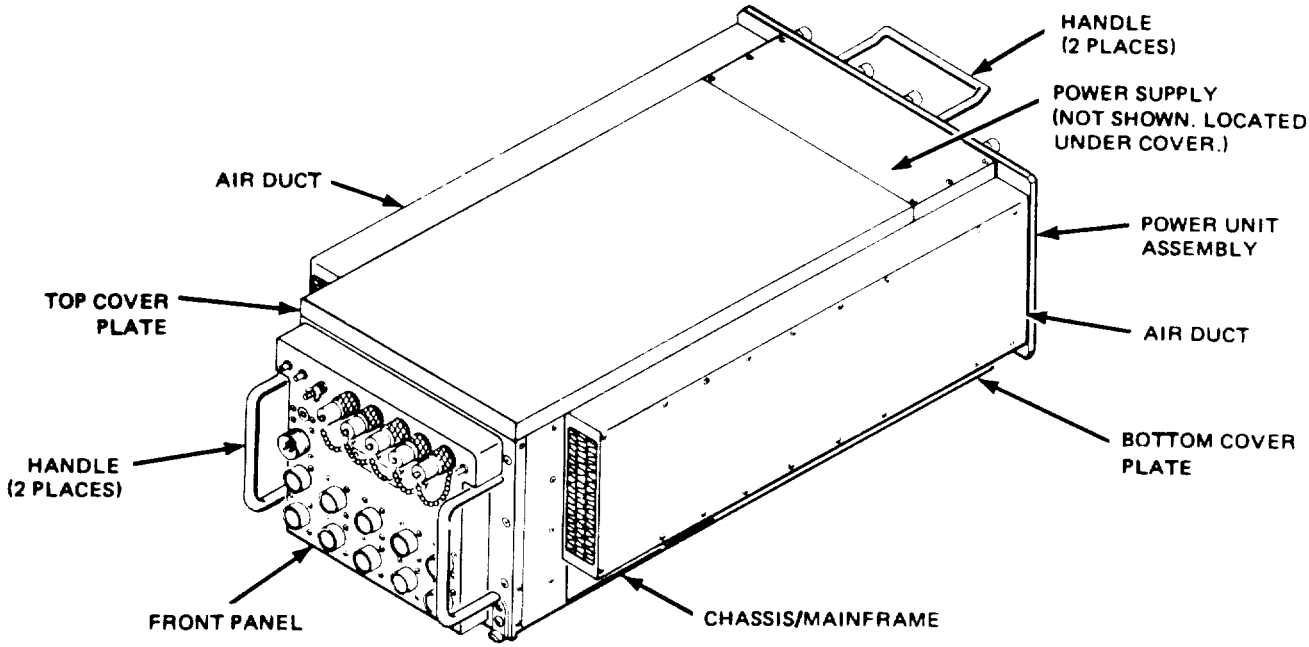
1-12. EQUIPMENT CONFIGURATIONS

The paragraphs to follow discuss the versions of the processor and the system configurations in which the processor may be deployed.

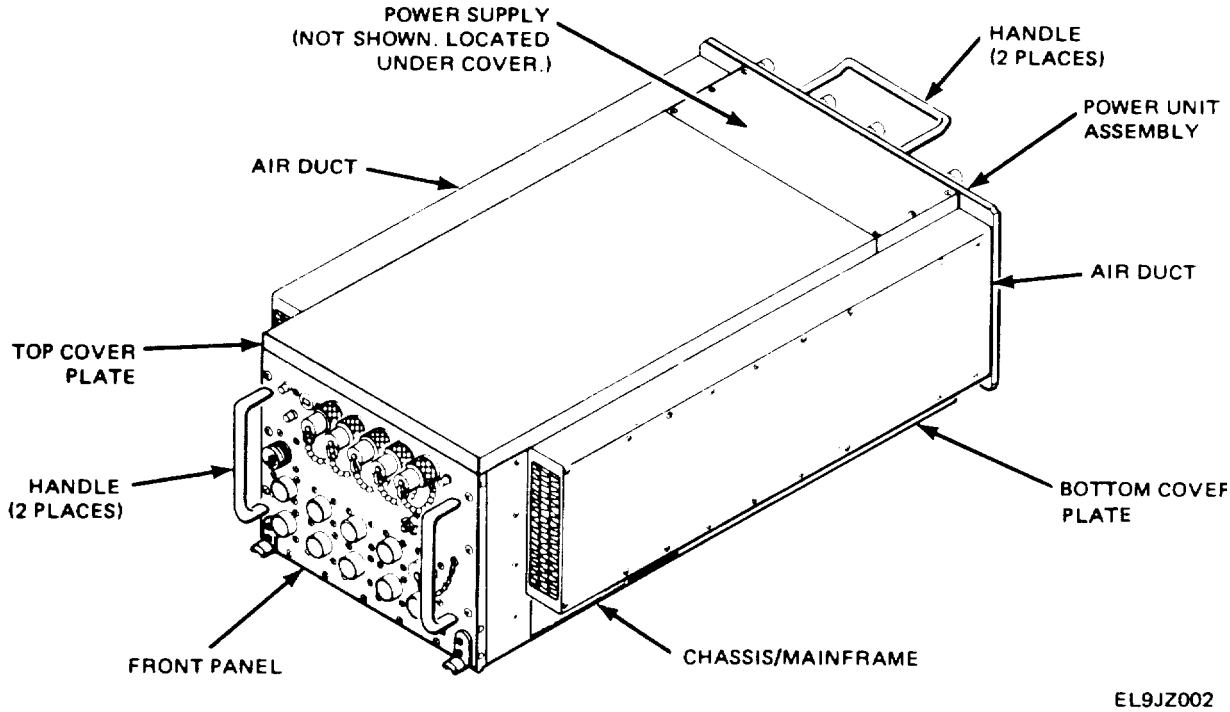
a. Processor Configuration. The primary differences between one version of the processor and any of the other seven versions are (table 1-4 and fig. 1-7, 1-8, 1-9, 1-10):

- Type of power system (ac or dc)
- Type of memory (core or semiconductor)
- Model of CPU PROM PCB (P/N 109836-01 or 109836-04)
- Model of FPU-C PCB (FPU-CE, P/N 109836-01 or FPU-C66, P/N 110984-01)
- Model of Motherboard Assembly (P/N 109884-01 or P/N 109885-02); includes Front Panel Assembly
- The chassis configuration (P/N 110393-02 or 110815-02)
- Type of I/O PCBs (Appx C, D, and E)

Of prime interest when considering processor configurations (versions) is the card cage. The paragraph to follow discusses the configuration of the processors' card cage.



CORE-BASED PROCESSOR



SEMICONDUCTOR-BASED PROCESSOR

Figure 1-1. Semiconductor-Based and Core-Based Processors, Component Locations

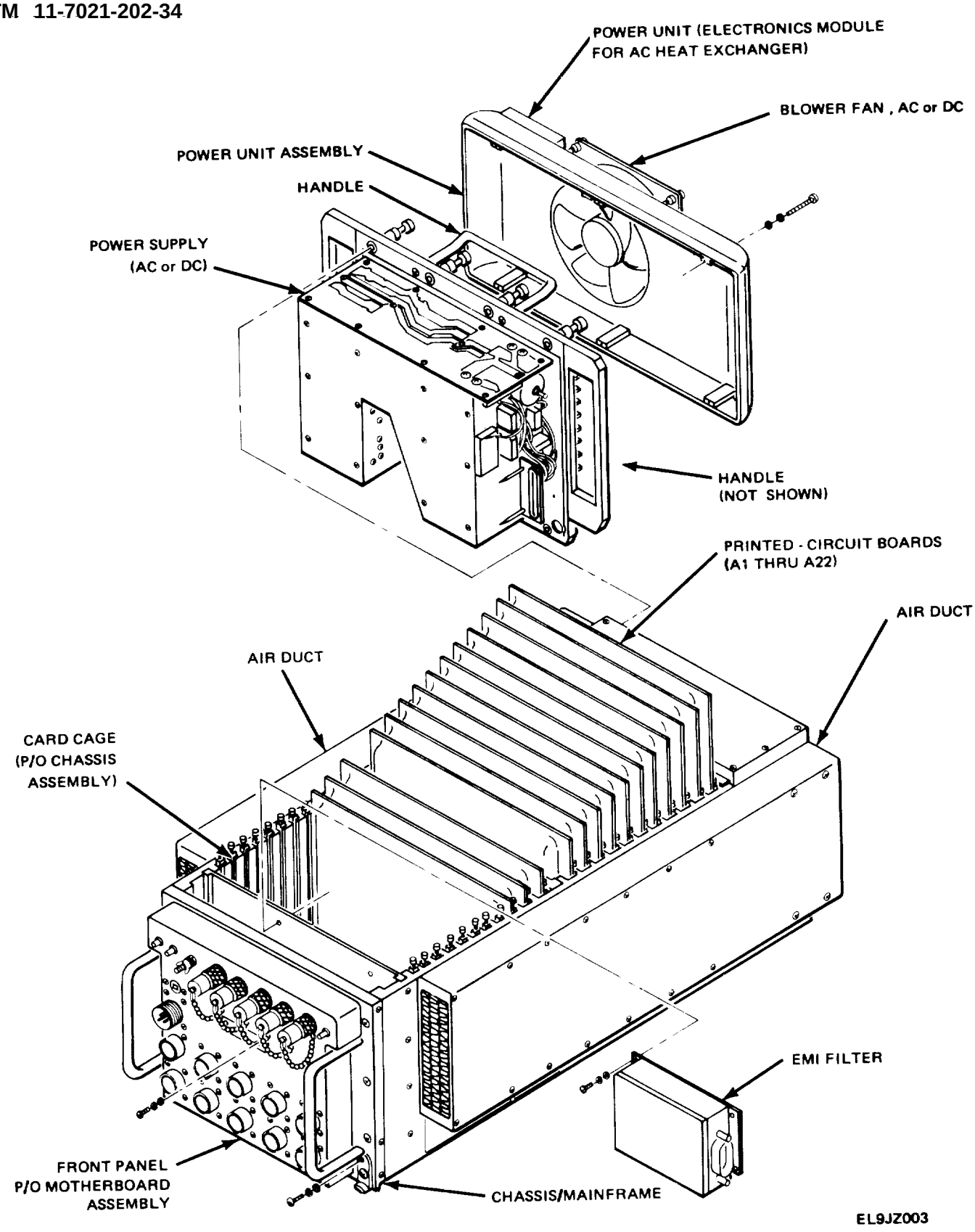


Figure 1-2. Processor Major Components, Front Oblique View

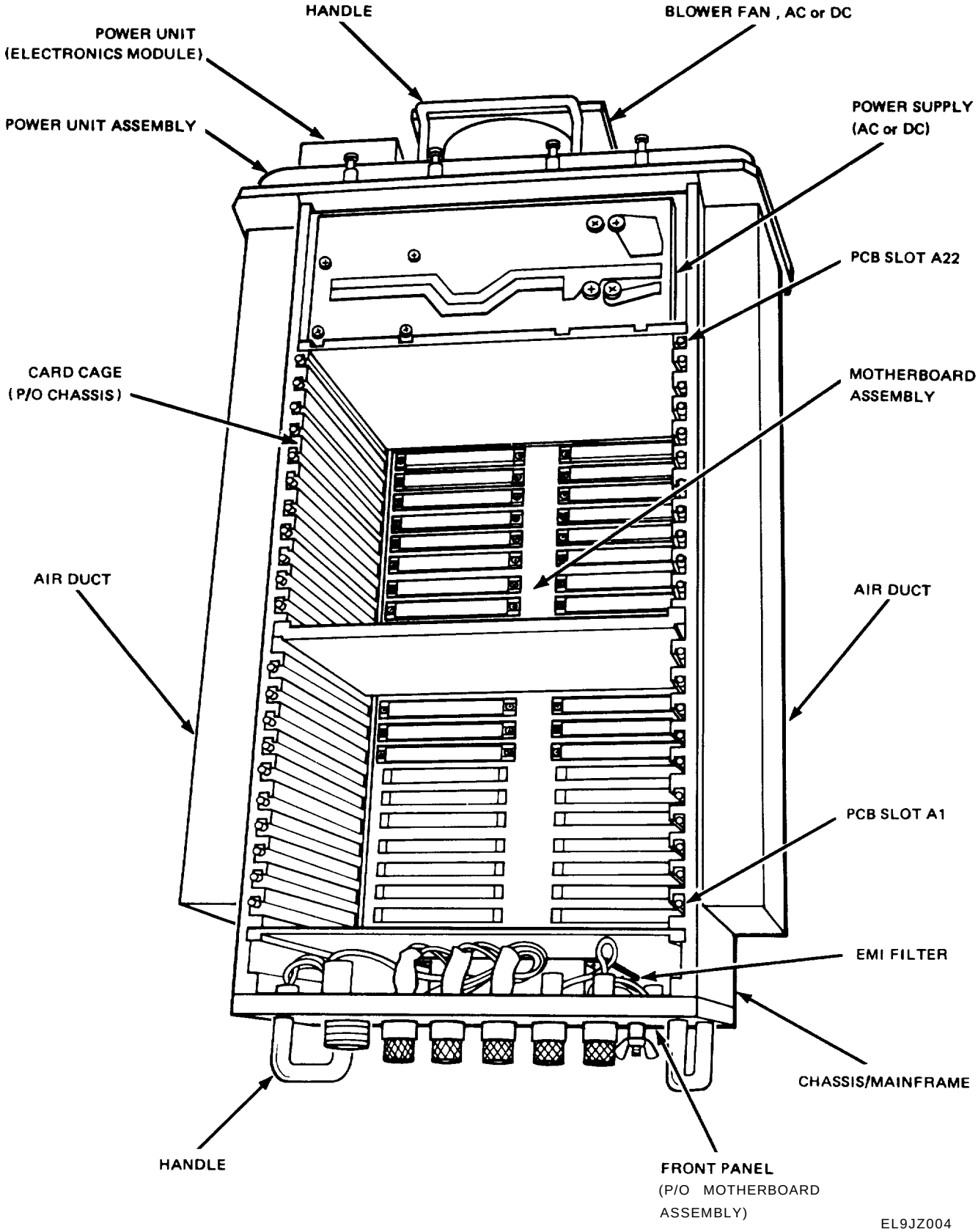


Figure 1-3. Processor Major Components, Top Cover Plate and PCBs Removed, Top View

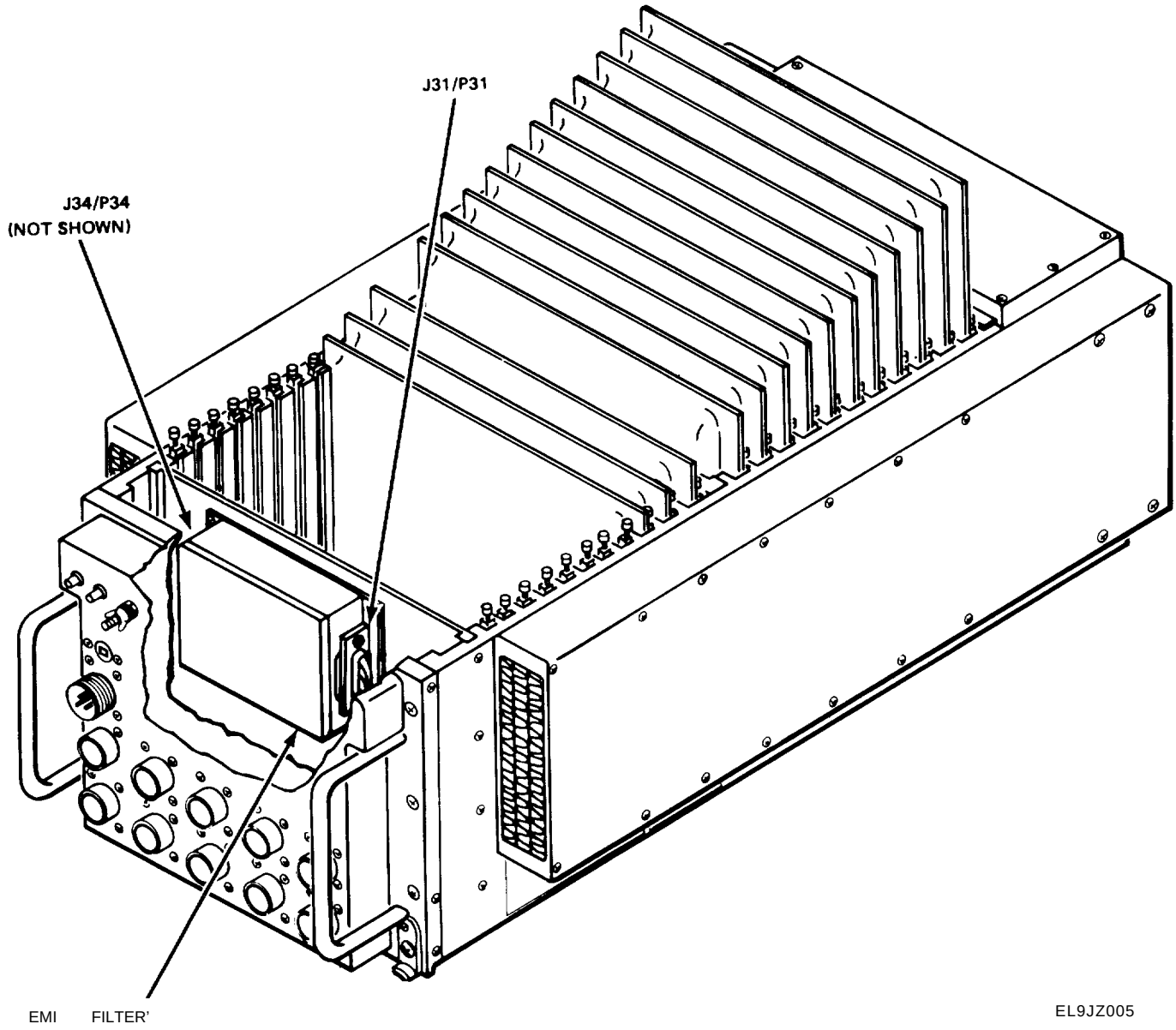
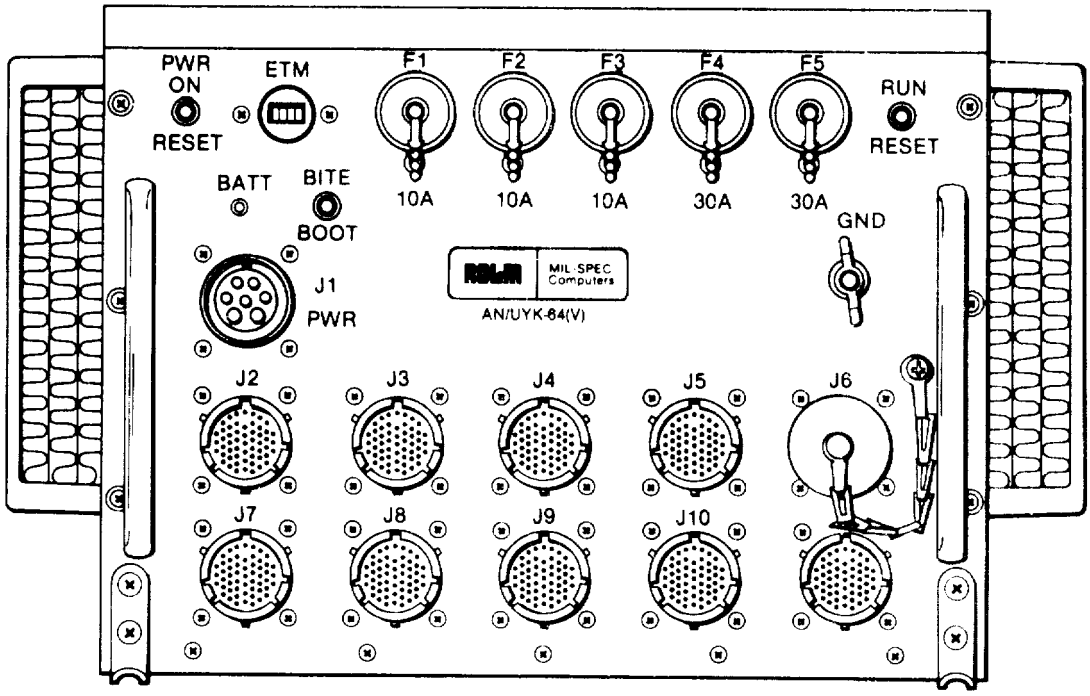
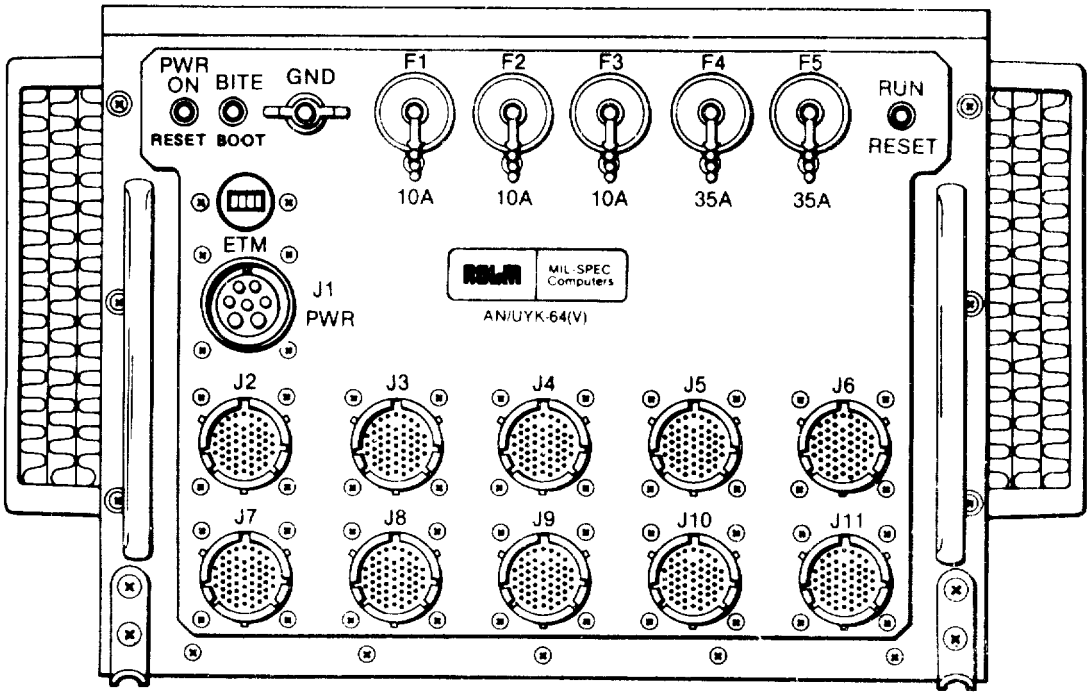


Figure 1-4. Location of EMI Filter

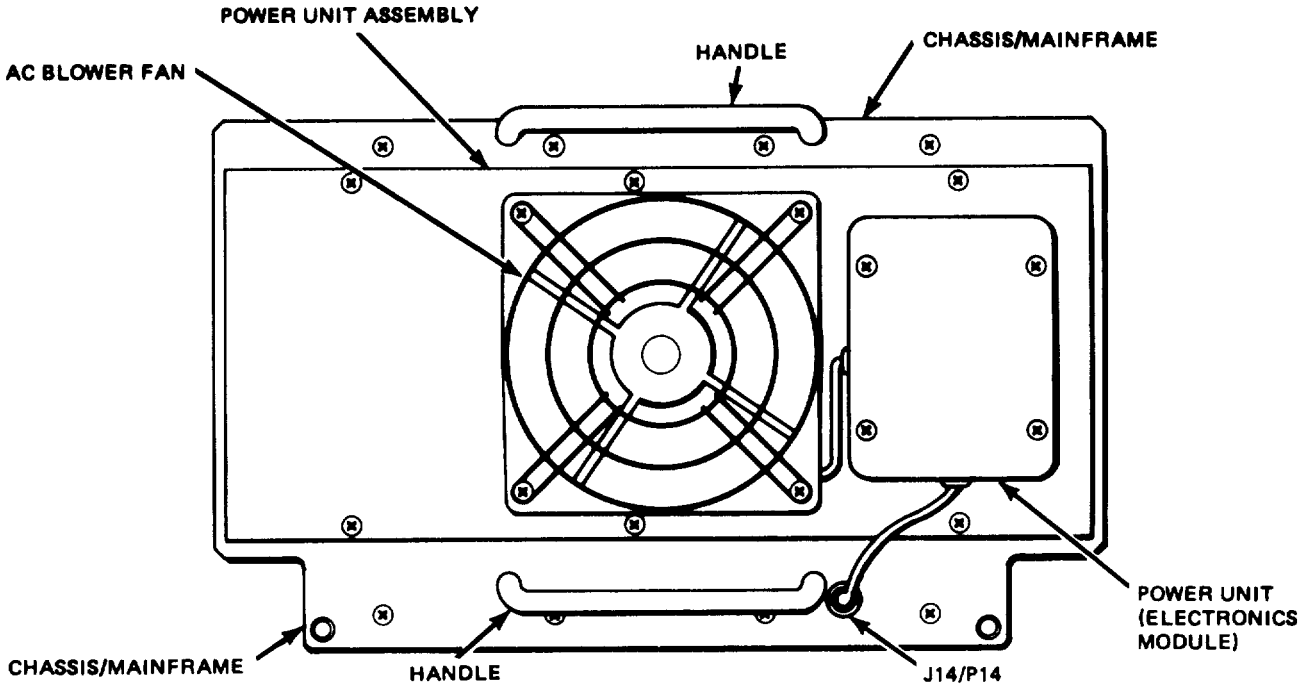


SEMICONDUCTOR-BASED PROCESSOR {V1, V1X, V3,V3X)

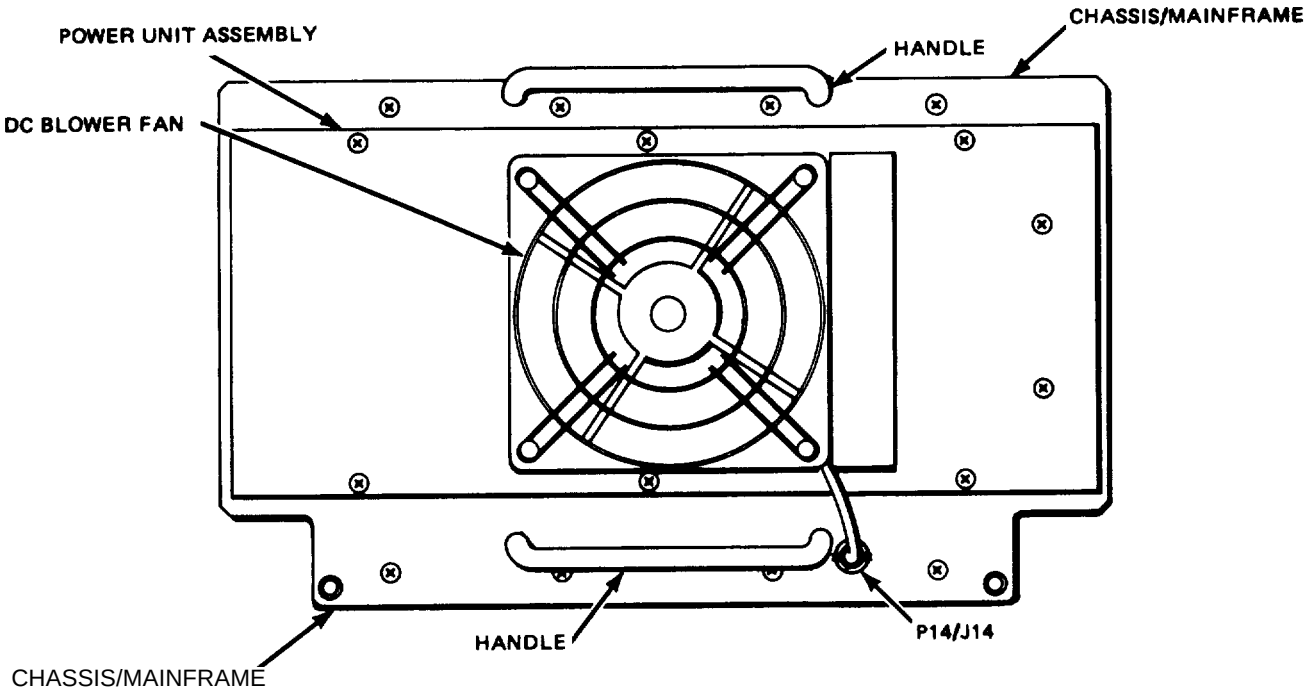


CORE-BASED PROCESSOR (V2, V2X, V4, V4X)

Figure 1-5. Processor Core and Semiconductor Front Panels



AC POWER UNIT ASSEMBLY (V1, V2, V3, V4)



DC POWER UNIT ASSEMBLY (V1X, V2X, V3X, V4X)1

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Figure 1-6. AC and DC Power Unit Assemblies, Rear View

Table 1-3. Front Panel Connectors, Indicators, Controls, and Fuses

Item	Function
PWR ON/RESET Indicator	Indicating pushbutton switch. Indicates when prime power is applied; excluding battery back-up in a AN/UYK-84(V)1, 1X, 3, or 3X chassis. Pushbutton resets power after power has been interrupted.
ETM Display (Elapsed Time Meter)	Numerical display. Shows the accumulated time the processor has been running (power application); excluding battery back-up operating time in the processor 1X, V3, or V3X chassis. Elapsed time is shown in hundreds of hours, plus first place decimal.
BATT Indicator	LED indicator. The indicator is lit to signify that the $5 V memory bus is up; V1, 1X, 3, 3X only.
BITE/BOOT Indicator	Indicating pushbutton switch. Indicator is lit to signify that BITE self-testing was successful the last time it was executed. The pushbutton is also used to load (boot) the operating program from a dedicated external device.
RUN/RESET Indicator	Indicating pushbutton switch. Indicates when a program is running. Pushbutton is used to reset operating system and reinitialize the processor.
F1, Fuse Assembly	10 ampere, normal-blo fuse; phase A leg of primary ac power wiring.
F2, Fuse Assembly	10 ampere, normal-blo fuse; phase B leg of primary ac power wiring.
F3, Fuse Assembly	10 ampere, normal-blo fuse; phase C leg of primary ac power wiring.
F4, Fuse Assembly	For core memory processors: 35 ampere, AGC 35 fuse. For semiconductor memory: 30 ampere, AGC 30 fuse. Part of the $28 V power wiring.
F5, Fuse Assembly	For core memory processors: 35 ampere, AGC 35 fuse. For semiconductor memory: 30 ampere, AGC 30 fuse. Part of the -28 V power wiring.

Table 1-3. Front Panel Connectors, Indicators, Controls, and Fuses — Continued

item	Function
J1, 7-Pin PWR	Power input connector used to connect externally supplied ac and dc voltages, plus system grounding.
J2, 55-Pin I/O Connector	Provides I/O interface between I/O PCB A1 and the external system.
J3, 55-Pin I/O Connector	Provides I/O interface between I/O PCB A2 and the external system.
J4, 55-Pin I/O Connector	Provides I/O interface between I/O PCB A3 and the external system.
J5, 55-Pin I/O Connector	Provides I/O interface between I/O PCB A4 and the external system.
J6, 8-Pin Battery Connector (AN/UYK-64(V)1 1x, 3, 3x	Connects a remote back-up ± 28V battery supply for semiconductor memory configurations.
J6, 55-Pin Memory Connector (AN/UYK-64(V)2, **2x,** 4, 4x	Connects a remote memory for the expansion of memory in the core memory configurations.
J7, 55-Pin I/O Connector	Provides I/O interface between I/O PCB A5 and the external system.
J8, 55-Pin I/O Connector	Provides I/O interface between I/O PCB A6 and the external system.
J9, 55-Pin I/O Connector	Provides I/O interface between I/O PCB A7 and the external system.
J10, 55-Pin I/O Connector	Provides I/O interface between I/O PCB A8 and the external system.
J11, 55-Pin System Terminal Connector	Provides system terminal command and control, between the processor and the system terminal.
GND Wing-Nut Stud	Provides a chassis ground connection capability.

Table 1-4. Processor Configuration Matrix

Assembly Number/ Model Description	Processor Configurations							
	V1	V1X	V2	V2X	V3	V3X	V4	V4X
PROCESSOR ASSEMBLY:								
112261-03	x							
112261-07		x						
112260-03			x					
112260-07				x				
110991-05					x			
110991-11						x		
110991-05							x	
110991-11								x
MOTHERBOARD ASSEMBLY:								
109883-02	x	x			x	x		
110800-02			x	x			x	x
CHASSIS ASSEMBLY:								
110393-02	x	x			x	x		
110815-02			x	x			x	x
POWER SUPPLY:								
112676-01 (5687) DC Power		x		x		X		x
113081-01 (3884) DC EMI Filter		x		x		x		x
110684-01 (5617) AC Power	x		x		x		x	
112241-01 (3883) AC EMI Filter	x		x		x		x	

Table 1-4. Processor Configuration Matrix-Continued

Assembly Number/ Model Description	Processor Configurations							
	V1	V1 x	V2	V2X	V3	V3X	V4	V4X
CORE MEMORY:								
109848-01 (1755) Controller	---	---	**x**	x	...	---	**x**	x
109550-01 (2019) Memory	-..	. -	**x**	**x**	...	-..	x	x
SEMICONDUCTOR MEMORY:								
109844-01 (1753) Controller	x	x	.-.	...	x	x	---	..-
109840-01 (2030) Memory	x	x	...	-..	x	x	-..	.-.
109852-01 (1754) ERCC Controller	x	x	---	.-.	x	x	.-.	...
FLOATING POINT UNIT:								
109856-01 FPU-A	x	x	x	x	x	x	x	x
109860-01 FPU-B	x	x	x	x	x	**x**	x	x
110984-01 FPU-C66	x	x	x	x	---	.-.	.-.	---
100941-01 FPU-CE	.-.	...	...	...	x	x	x	x
CENTRAL PROCESSING UNIT:								
109824-01 DATA	x	x	x	x	x	x	x	x
109828-01 PFP	x	x	x	x	x	x	x	x
109836-04 PROM	x	x	x	x	---	- .	..-	.-.
109832-01 MAP	x	x	x	x	x	x	x	x
109836-01 PROM	.-.	.-.	---	.-.	x	x	x	x

INPUT/OUTPUT: — Refer to Appendix G.

b. Card Cage Configuration. The Processor's card cage consists of the core or semiconductor memory section, FPU section, CPU section, and the I/O section (fig. 1-7, 1-8, 1-9, 1-10).

Although the card cage contains eight I/O board slots, the type of I/O boards used can vary considerably, according to the number and type of peripheral devices required in a specific system configuration (Appx E).

c. Memory Configuration. The following subparagraphs discuss the processor memory configurations.

(1) Semiconductor Memory. The memory size in a semiconductor-based processor is 256k Words. The word length is 21 bits, consisting of 16 data bits and a 5-bit error correction code, The 5-bit error correction code is generated by the A16 ERCC PCB during a memory-write cycle and is checked during a memory-read cycle. The memory cycle time is increased only if an error is corrected. The error code is transparent to the CPU. Semiconductor memory is volatile and cannot retain data integrity when there is a power interruption of up to 60 minutes,

(2) Core Memory. The memory size in a core-based processor is 64k Words. The word length is 17 bits, consisting of 16 data bits and an odd parity bit. The A16 lMC/RMC controller PCB controls both internal and external memory. Core memory is non-volatile and retains data integrity for an indefinite duration, even with loss of prime power to the processor.

Core memory size can be increased in 32k word increments; however, increases above the already contained 64k words requires the addition of, and interfacing of, one or more remote memory chassis (via J6).

d. System Configuration Refer to appendix E for processor system configuration information.

1-13. SAFETY PRECAUTIONS

The processor is a heavy piece of equipment. Three technicians are employed when moving the unit. Handles are provided on the processor as an aid when moving the processor. Use them (fig. 1-3).

A periodic review of safety precautions in TB 385-4, Safety Precautions for Maintenance of Eiectrical/Electronic Equipment, is recommended, When the equipment is operated with covers removed, DO NOT TOUCH exposed connections or components. MAKE CERTAIN you are not grounded when making connections or adjusting components inside the test instrument.

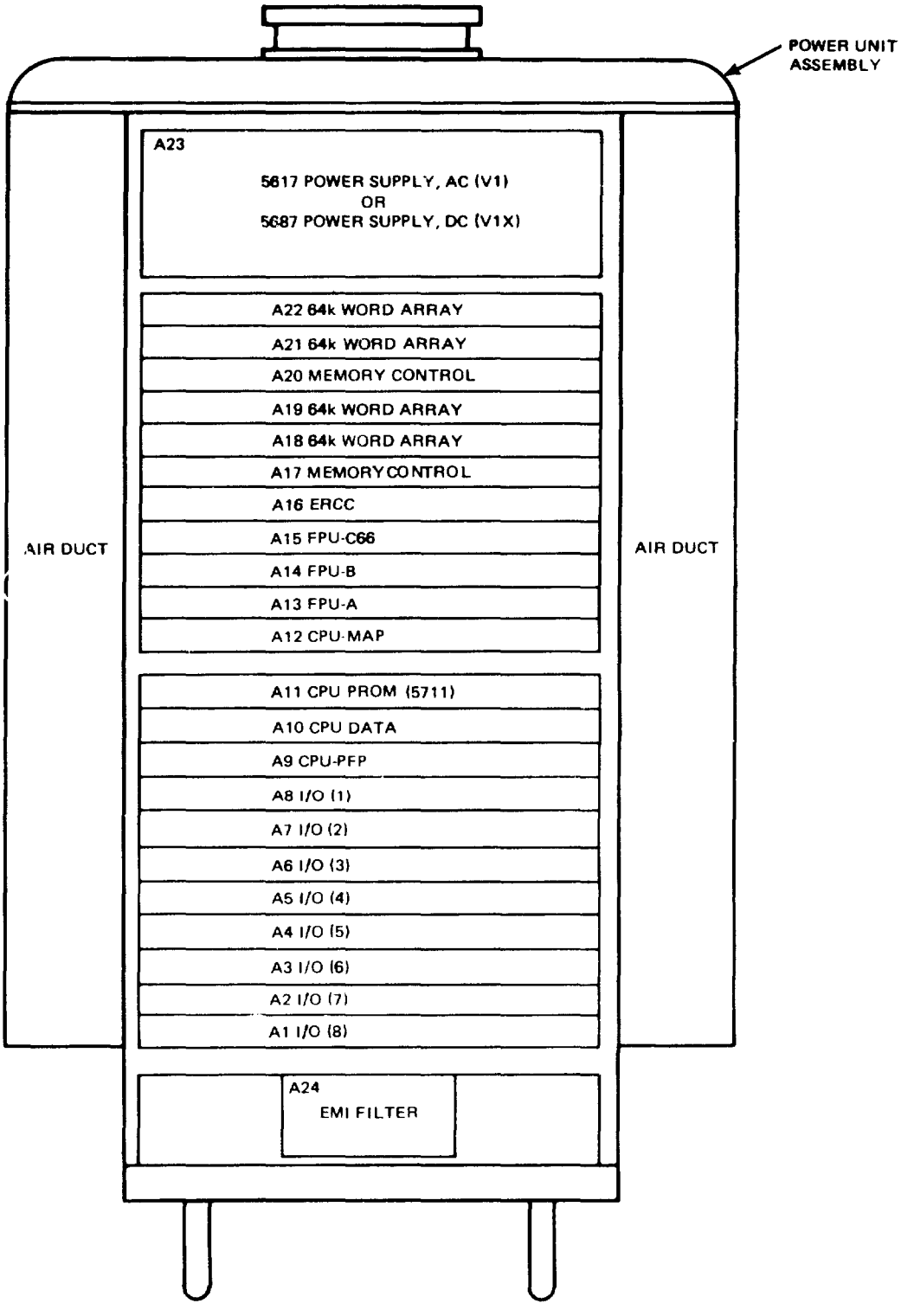


Figure 1-7. Processor Chassis Configurations V1,V1X

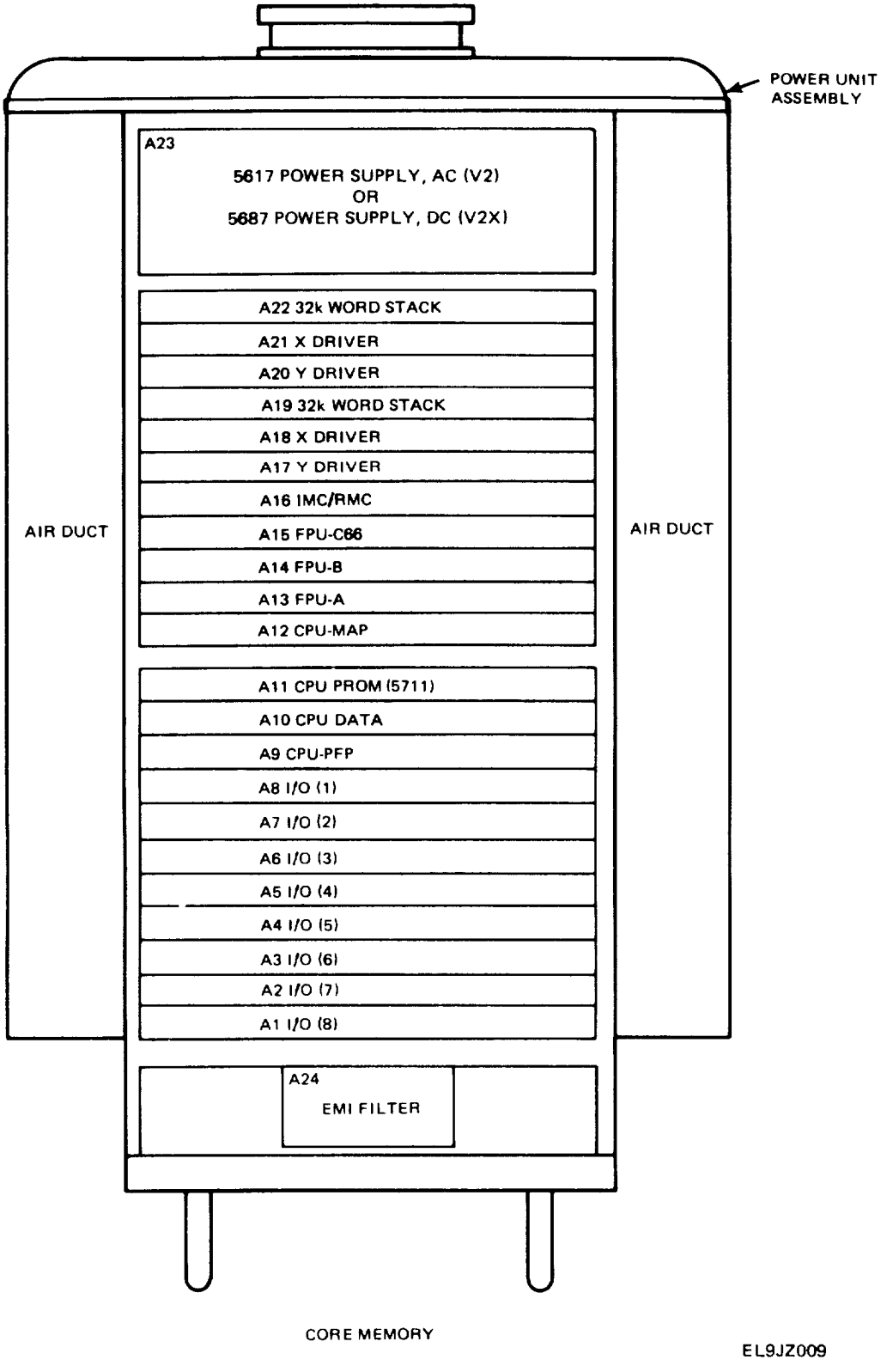


Figure 1-8. Processor Chassis Configuration, V2, V2X

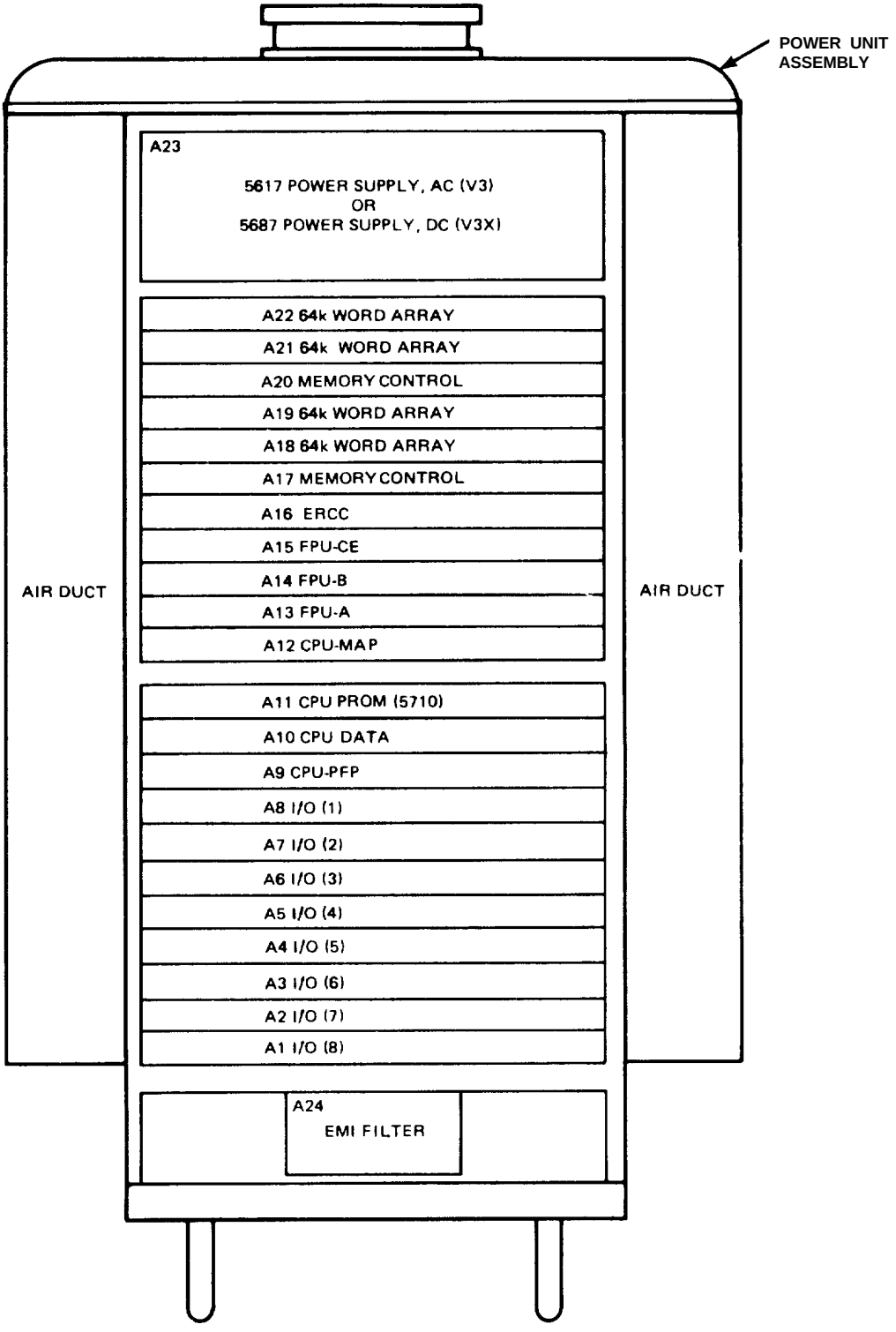


Figure 1-9. Processor Chassis Configurations V3, V3X

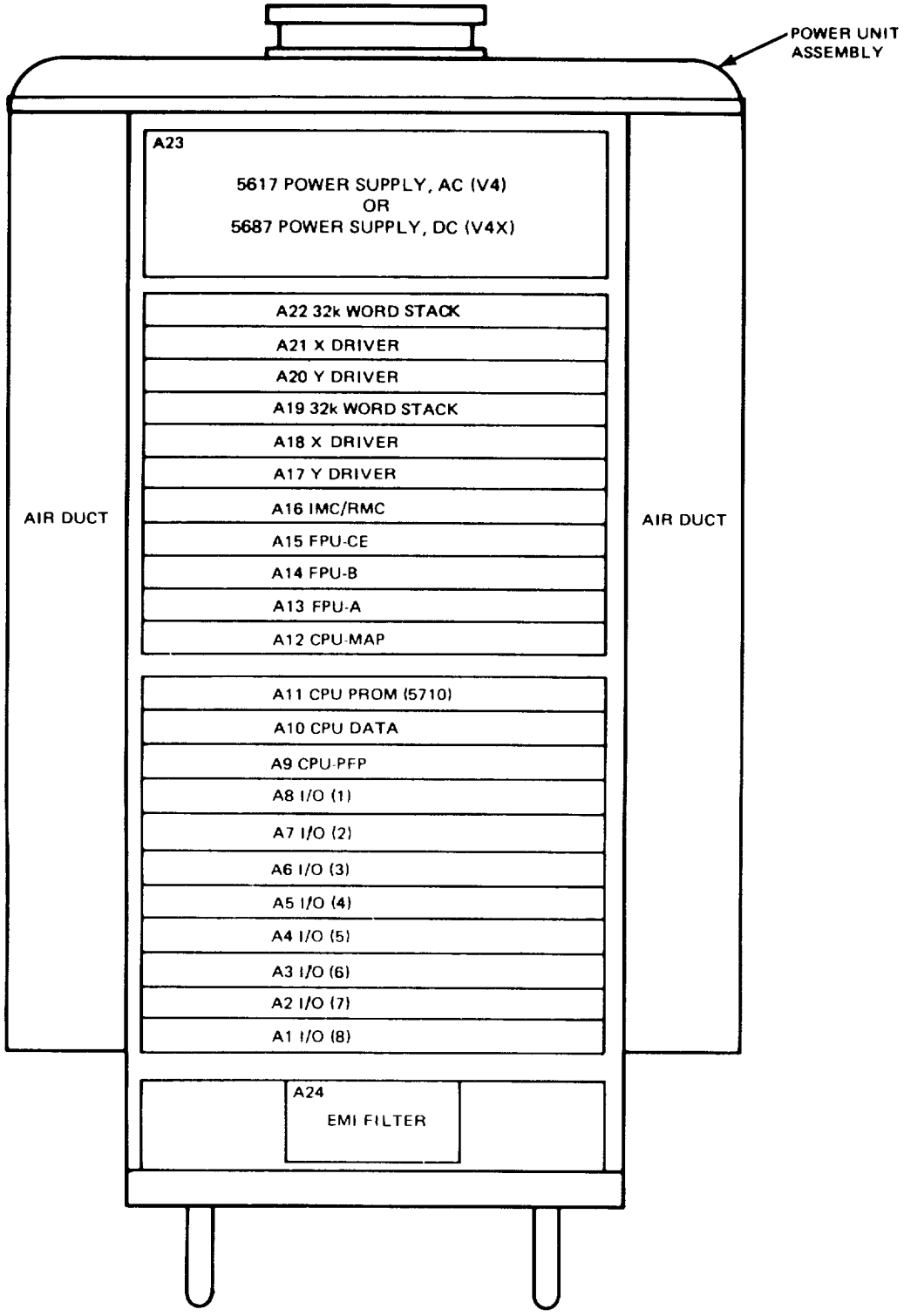


Figure 1-10. Processor Chassis Configurations, V4, V4X

Section III. PRINCIPLES OF OPERATION

1-14. INTRODUCTION

The principles of operation for the Processor are presented as follows:

- Functional overview
- Central processing unit (CPU)
- Floating point unit (FPU)
- Core memory
- Semiconductor memory
- Power supplies (ac and dc)
- Internal electrical connections

Configuration and interface information is contained in appendices C, D, and E.

1-15. FUNCTIONAL OVERVIEW

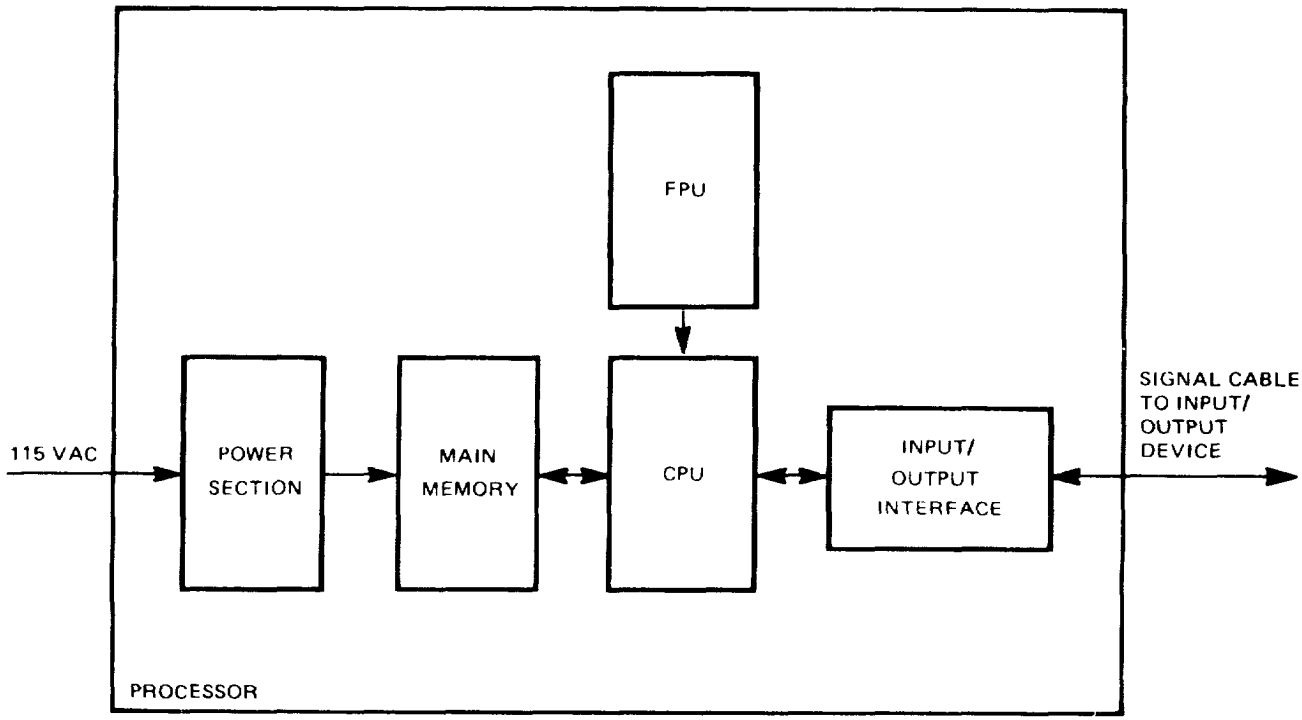
The processor is functionally divided into five subsystems (sections): power; memory, either core or semiconductor based; floating point unit (FPU); central processing unit (CPU) and; input/output(I/O); (fig. 1-1 1).

CPU. The central processing unit (CPU) consists of four printed circuit boards (PCBs). It decodes and initiates execution of all instructions, and performs all fixed-point arithmetic and memory reference operations. Its principle functional components are the arithmetic logic unit (ALU), and its input and output bus; the prefetch processor (PFP) and its bus; the asynchronous communications interface for the system terminal; and The memory bus interfaces.

b. Memory. Main memory is either core or semiconductor based. The core memory size is 64 kB and contained within the processor chassis; however, core memory can be expanded outside the chassis. The semiconductor memory size is 512 kB and contained within the processor chassis. Memory allocation and protection (MAP) is provided by the CPU and respective memory controllers.

c. FPU. The floating point unit (FPU) consists of three PCBs. The FPU performs floating point arithmetic on data supplied by the CPU and/or data in the internal floating point accumulators. Data transfers to and from the FPU are controlled by the CPU, which also instructs the FPU as to the type of operation to be performed. The actual execution of the arithmetic is independent of the CPU. The FPU is monitored by the CPU to determine when the operation has been completed, and when the result is available. The FPU does not have direct access to memory.

d. I/O Section. The input/output section is made up of processor slots A1 through A8. interface modules (PCBs) are installed in these slots to allow the processor to interface with other equipment. Refer to appendix G for additional I/O information.



NOTE FOR DC OPERATION, AC EMI FILTER (3683) AND POWER SUPPLY (5617} IN PROCESSOR ARE REPLACED BY DC EMI FILTER (3884) AND DC POWER SUPPLY {5687).

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Figure 1-11. Simplified Functional Block Diagram of the Processor

e. Power Section. The power section supplies the necessary power to run the processor. It operates from either 115 V ac, 47 to 440 Hz, using an ac EMI filter and power supply, or from 24 or 32' V dc using the dc EMI filter and power supply. Fuses F1, F2, and F3 give overload protection when the processor is set up for ac. Fuses F4 and F5 are used for dc overload protection.

f. Major Subsystems and System Buses. A typical system configuration has two principal internal buses; memory in (MEMIN), memory out (MEMOUT), and one principal external bus; the I/O bus.

The two internal buses handle all data exchanges between the subsystems. The MEMIN bus carries address and write data to the memory system and also carries information from the CPU to the FPU. The bus is unidirectional, and is 21 bits wide, permitting physical addressing of 1024k words in core memory systems, and the transfer of 16-bit data words in both semiconductor and core memory based systems. The MEMOUT bus is essentially a 16-bit unidirectional bus, carrying data and instructions read from memory to the CPU; programmed I/O information and data from the CPU to the FPU; and floating point information from the FPU to the CPU. The I/O Bus, under CPU supervision, interfaces with both memory buses for the purposes of direct memory access and I/O transfers.

The I/O bus carries all command and data transactions between the processor and system peripheral device interfaces. There are two types of transactions: Programmed I/O and direct memory access (DMA). Programmed I/O operations are initiated by the CPU to execute a software instruction. The operation may involve a transfer of data to or from an I/O interface, the transmission of a control command from the CPU to the device including functional parameters, or the retrieval of the device status.

DMA operation is initiated by the CPU, but involves the transfer of data between the I/O interface and memory without CPU intervention. For both programmed I/O and DMA transfers, 16 bidirectional data lines within the I/O bus are used. The remaining 5 lines within the bus are used for control and device selection functions. I/O bus protocol is described in appendix C, D, and E. The system terminal is connected to the universal asynchronous receiver/transmitter (UART) in the CPU by a communications line (RS-232C).

The CPU coordinates the operations of all the other subsystems and control lines. The CPU executes all memory data references and instruction fetches by means of its mapping logic, which translates a 15-bit logical address into a 20-bit physical address, places the address on the MEMIN bus, and requests the appropriate memory cycle.

The MAP logic checks for protection violations. If a violation is detected, the CPU is notified and a protection trap ensues. If the memory cycle involves a write-to-memory, the CPU places the data on MEMIN within specified timing constraints. If a memory-read-operation is involved, as in the case of an instruction fetch, the memory places the data on the MEMOUT bus and the CPU takes the data from the bus.

After the CPU has received the data from an instruction fetch, the instruction is decoded and the appropriate action is taken. If the instruction requires memory references, the CPU will execute them, Accumulator-to-accumulator operations, including fixed-point arithmetic, are executed entirely with the CPU.

g. Bus Utilization. The following paragraphs describe data and information between the major subsystems and how these exchanges are effected on the system buses.

Floating-point arithmetic instructions involve both the CPU, and the FPU for their execution. The CPU determines the status of the FPU by retreiving the FPU status word on the MEMOUT bus. The status is changed by the CPU and sent to the FPU on the MEMIN bus. While memory buses are being used in this fashion, memory reference cycles are inhibited. When the CPU provides the operands, they are transferred to the FPU on the MEMIN bus. When the memory provides one or both operands, they come from memory on the MEMOUT bus and transferred to the FPU using the CPU and not the FPU to provide the memory address. When required by the CPU, the result is transferred from the FPU to provide the memory address. When required by the CPU, the result is transferred from the FPU on the MEMOUT bus. If the result is to be stored in memory, the memory address (MEMIN) is supplied by the CPU with the result supplied by the FPU (MEMIN). The actual instruction and control signals are transferred directly from the CPU to the FPU on dedicated instruction lines. The FPU does not have direct access to memory, All memory addresses required during a floating point arithmetic operation are provided by the CPU, not the FPU.

During output operations (I/O), the 16 bidirectional lines of the I/O bus are an extension of MEMOUT in the one direction. During input operations MEMIN is an extension of the 16 data lines in the opposite direction.

The CPU sends commands during programmed I/O operations (output), control functions, and data to the device via the I/O bus and I/O interface. During data transfers, the CPU first reads the data from memory into an accumulator, then transfers the data from the accumulator to the I/O interface.

During input operations, the CPU receives data and status information from the device via the I/O interface I/O bus in response to a previously issued command. Data or status information is read into an accumulator. Status information is processed by the CPU to determine what course of action to take, according to the device service routine.

Before a DMA operation takes place, the device is given the starting address of a memory data buffer, to or from which data is to be transferred; the number of words or bytes to be transferred; and finally, the operational command. This functions the same as the programmed I/O, as it relates to the particular service routine. The information is obtained from memory by the CPU (MEMOUT) and sent from the CPU to the device via the I/O bus and I/O interface. Once the DMA operation commences, memory addresses are supplied by the device and appear on MEMIN. The direction of data flow depends on the operation being performed. For example: When a write command is issued to a magnetic tape unit, data is read from memory as if there was a direct path from memory (MEMOUT) to the tape unit. When a read command is issued, data is read from the tape and written into memory (MEMIN), again as if there was a direct data path. The I/O device supplies the memory address by using increments of the start address.

1-16. CENTRAL PROCESSING UNIT (CPU) DESCRIPTION

The CPU is microprocessor based and microprogram controlled. There are four PCBs, identified by function rather than alpha or numeric designators: the PFP board; the PROM board, which controls the microprogram and its address sequencing; the data board, which handles data flow and arithmetic logic unit ALU operations, and the map board which contains the the MAP board which contains the memory allocation and protection logic to translate a logic address into a physical address.

a. Internal Buses and Data Flow. The following paragraphs describe the flow of data within the CPU, to and from the microprocessor, and on the buses.

(1) ALU In Bus (ALUIN, 0-15). The 16-bit ALU in bus provides the data inputs (D inputs) to the microprocessor. The immediate source of the inputs varies according to the type of operation being performed. For example, data read from memory to the CPU is clocked into the memory out register and then gated onto ALUIN. Input sources to ALUIN include: UART, which provides eight data bits; byte swap logic, which transposes the byte positions in a data word; I/O data bus, which has an interface to ALUIN for transferring data during a programmed I/O operation; and MAP logic, for the purpose of reading the contents of the MAP. Other input sources are the prefetch processor (PFP), providing a means of reading one of the program counters; the register stack; the console PROM interface; and the effective address sign extend logic,

(2) ALU Out Bus (ALUOUT, 0-15). The bit ALU out bus carries the data outputs (Y-outputs) from the microprocessor to a number of immediate destinations during the course of a memory write cycle, These destinations from ALUOUT include: the Memory in register, UART, byte swap logic, the I/O data bus; map logic; the PFP; register stack; and the console PROMS.

(3) Prefetch Processor Bus (PFP, 0-15). The 16-bit PFP bus links the functional elements of the prefetch processor. It provides a path from the PFP Instruction storage Register to the instruction register (IR) and the microprogram control logic. It provides inputs to the decode ROM, start address generator (SAGE), and ALC decode logic. Their function is to provide an initial address to control memory according to the type and group of the instruction about to be executed. In addition, the PFP bus provides gated inputs to the ALUIN bus, for such purposes as monitoring the instruction storage register. The ALUOUT bus provides a buffered input to the PFP bus so that the CPU can load the PC and alter the microcode flow, as required.

(4) Control Memory Address Bus. This is a 12-bit bus (CMEMADR, A, 0-10) that provides the microprogram control memory with a cell address. Depending on the function being performed, the address may be provided by the microsequencer, decode ROM, the SAGE logic, or from control memory itself. The address determines the next step to be taken in execution of the instruction.

(5) Memory In-In Bus (MEMININ, 0-5, 16-19). MEMININ bus provides an indirect input to the MEMIN bus. The 10-bits are derived from the MAP RAM. In conjunction with ALUOUT6-15 they form a 20-bit physical address. A partial input to the memory in register and the PFP program counter comes from the MEMININ bus. It also provides a buffered input to the ALUIN bus so that the CPU can read the MAP contents.

(6) FPU Control Bus. The FPU control bus consists of 15 instruction bits derived from the CPU instruction register. The FPU uses the nine most significant bits, and nine control lines. Five of the nine control lines are from CPU to FPU and the remaining four lines are from FPU to CPU. The significance of the control lines is described in later paragraphs concerning the FPU.

b CPU Microprocessor. The microprocessor consists of four 2901 4-bit microprocessors configured as a 16-bit microprocessor (U1, U2, U3, and U4 on the CPU data board). The D-inputs are derived from the corresponding 4-bit segment of ALUIN. The Y-outputs are gated onto the corresponding bit positions of ALUOUT. The microprocessor and ALU functions are controlled from U46, U47, and U48 of the microinstruction register (UIR).

A-Register and B-Register select bits are derived from UIR bits 8-11 and UIR bits 13-16, respectively. The A-Register can only be specified as a source in ALU functions. The B-Register can be specified as either a source or destination.

ALU functions and operations are specified by UIR bits 26, 17, 18, 19, 20, 21, and 22, Bit 26 is the carry input to the ALU. Bits 17, 18, and 19 are the function select bits. Bits 20, 21, and 22 are the source select bits. The ALU function is expressed as a 3-digit octal number. The first digit is bit 26. Bits 17, 18, and 19 are the second digit. Bits 20, 21, 22 are the third digit. The operands are identified as A, B, D, Q, and Z, as follows:

A = A-register field

B = B-register field

D = 2901 D-input ports (ALUIN)

Q = 2901 internal Q-register

z = Zero operand

A notted signal name means that the operand is inverted (e,g., A is the inverse or one's complement of A).

The destination field is expressed by UIR bits 23, 24, and 25. The ALU outputs are internally multiplexed to the Y-outputs of the 2901.

c. General Purpose Registers. There are 16 general purpose registers in the CPU consisting of four 4 X 16 RAM chips (U5, U6, U7, and U8 on CPU Data board). The register inputs are derived from the ALUOUT bus and the register outputs are fed directly onto the ALUIN bus.

The registers are controlled by the particular microinstruction. A register address is determined by UIR bits 50-53. The registers are selected when RAND2 (lesser random field No.2) is low, and when the field decode is 6 or 7; i.e., when either R6 or R7 is low. A write function is specified (WRTRF) by R6. A read function is specified (RDRF) by R7. The write function (input) is synchronized by BUSEQCLKA, so that only the pertinent information on ALUOUT is written into the selected register during the sequence.

d. Byte Swap Logic. The byte swap logic consists of two buffers. When enabled, these buffers transfer the information on ALUOUT to ALUIN. Byte swapping is a feature of the UART service routine, since all CPU data transfers to or from the UART occur on the low order byte position (bits 8-1 5) of ALUOUT and ALUIN respectively.

e. Literal Field Register and Buffer. The literal field register and buffer (U53, U56 on CPU—data PCB) gates the microinstruction literal field onto ALUIN from the octal decode of the external source field of the microinstruction (CMEM 4, 5, 6). The literal field is represented by a combination of control memory (CMEM) bits, and microinstruction register (UIR) bits.

f. I/O Data Bus Drivers and Receivers. The I/O data bus is terminated on the CPU data PCB. The I/O data bus (DATAO-DATA15), is a negative true bidirectional bus, driven from ALUOUT during output operations and received on ALUIN during input operations. Refer to appendices C, D, and E for additional I/O information.

The I/O data bus receivers consist of two buffers, U62 and U64. The I/O data bus drivers consist of 16 nand gates in parallel, enabled by the decode of the microinstruction greater random field 2.

g. Universal Asynchronous Receiver Transmitter (UART). The UART is identified by the PCU as an internal I/O device, with non-maskable interrupt status. It is the principal component in the communications interface between the CPU and the system terminal. All the components of the communications interface, shown in block diagram form in figure 1-12 are installed on the CPU data PCB. The transmitted character may be up to 11 bits long, The present character format is one start bit, 8-data bits (without parity), and one stop bit. The format and baud rates are dependent upon the type of system terminal in use; e.g., CRT/keyboard, printer/keyboard, etc.

The line interface may be jumper connected for loop current operation or RS-232C operation. Jumpers W7, W2, and W4 are inserted for loop current operation via U44, and jumpers W3 and W6 are to connect U15 into the line circuit for RS-232C operation. Jumper W1 for all RS-232C baud rates, while W27 is inserted only for 110 baud.

The clock input to the baud rate generator is 2.5 MHz, derived from 5.0 MHz clock. The baud rate clock is selected from the 4-bit binary configuration of jumpers W17, W18, W19, and W20 as follows:

W17	W18	W19	W20	Baud Rate
1	1	o	1	50
1	1	0	0	75
0	0	0	0	110*
1	0	1	1	134.5
0	0	0	1	150
1	0	1	0	200
0	0	1	0	300
1	0	0	1	600
0	1	0	0	1200
0	1	0	1	1600
0	0	1	1	2400
0	1	1	0	4800
0	1	1	1	9600
1	1	1	0	19200

1 = Jumper inserted
0 = Jumper Omitted
* = Requires W27 Inserted

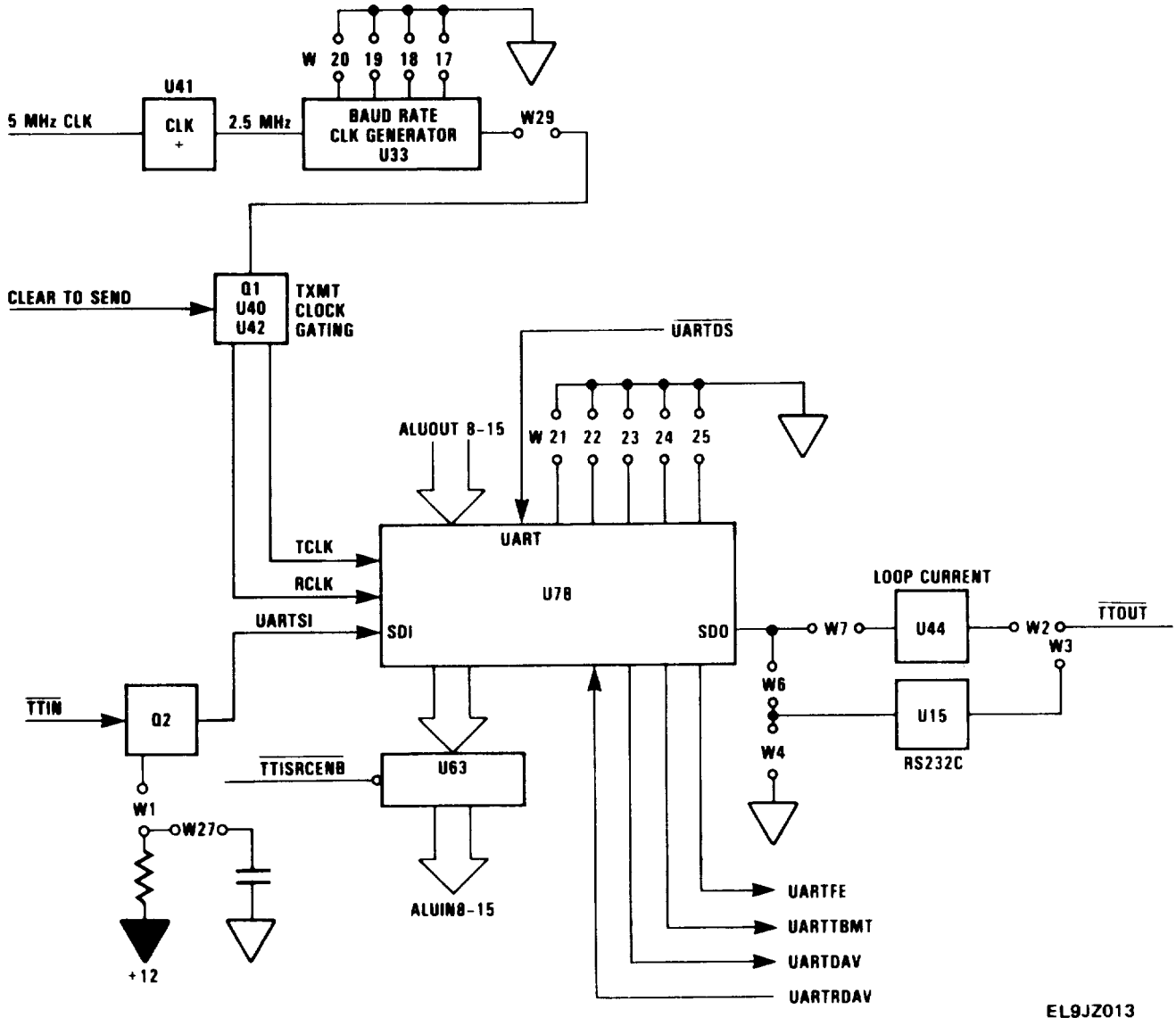

Figure 1-12. UART and Communications interface

The actual baud rate clock is 16 times the serial bit transmission rate (baud). W29 connects the clock output to the transmit clock/receive clock circuit. The Transmit Clock is inhibited if CLEAR TO SEND is low. The receiving device inhibits transmission from the UART when frequent character overruns occur at the receiving device. Transmit clock and and receive clock are generated unconditionally when CLEAR TO SEND is left open.

h. Microinstruction Format. The microinstruction is expressed in terms of control memory (CMEM) bits, which have a direct correlation to microinstruction register bits (UIR).

(1) Memory Control Field. The memory control field decode indicates a null, activates RQENB during a cycle, requests a memory READ, or requests a memory WRITE.

(2) External Source Field. The external field decode CMEM 4, 5 and 6 identifies the I/O data bus, the memory out bus, the external PC, the literal field, byte swap, short EFA, PFP bus, or a null.

(3) Shift Control Field. Shift control is also exercised by CMEM 4, 5, 6, when a shift function is specified by the ALU function field. Shift is effected internally by the ALU, and the forced inputs are determined by ALUR0, ALUQ0, ALUR16, AND ALUQ16.

(4) Greater Random Field 1. The greater random field 1 is specified by the combination of CMEM 27, 28, 29, and CMEM 56 signifying many things. It can signify No operation, an enabled PFP for prefetch, the floating-point processor, or that a memory reference is being initiated. It can also signify that there is a requirement to increment the PC at the end of the current microcycle; or it can call the decrement cycle counter, the floating-point processor control signal, or the load cycle counter.

(5) Greater Random Field 2. The greater random field 2 is specified by the combination of CMEM 27, 28, 29, and CMEM 47 which enables lesser random field 1, and the drive I/O data bus with ALUOUT.

(6) True and False State Changes. True state changes are specified by CMEM 30, 31, 32, and false state changes by CMEM 33, 34, 35. When USEQTEST is low UIR33, 34, 35 are decoded to determine the microsequence. When USEQTEST is high CMEM 30, 31, 32 are decoded to determine the microsequence. In addition, USEQTRUESTATE is low for true state changes and high for false state changes.

(7) Test Condition Select Field. There are 64 test conditions available to the microprogram, decoded by the hardware into eight groups of eight conditions each. The test group is decoded from UIR 36, 37, 38 with the requirement that USEQTRUESTATE is low and LITERALSRCENB is high. The particular condition within the selected group is decoded from UIR 39, 40, 41. The decode is effected by U44 on the CPU PROM PCB.

(8) Lesser Random Fields. The lesser random field decodes are enabled from the respective decodes of greater random field 1. The decode enable signals, RAND0 through RAND7, are generated accordingly. When CMEM 27 is high and CMEM 46 is low, CMEM 43, 44, and 45 are decoded (U53 on CPU PROM PCB) to provide the decoded signals R0 through R7. The combination of a decode enable (RAND0-RAND7) with R0-R7 effects the generation of the actual control bits.

(9) Microinstruction Register {UIR). The UIR consists of a number of latches that buffer the outputs of control memory. The UIR bits are derived directly from the corresponding CMEM bits. Not all CMEM bits are latched directly. Some are decoded by the field they represent and the decodes are latched, as is the case for the external source field, random field, and true state change field,

(10) Instruction Register (IR). The IR consists of two 8-bit latches, U55 and U56 on the CPU PFP PCB, that are clocked by IRCLK and loaded from the PFP bus. IR 0-15 corresponds to PFP 0-15, when the PFP bus represents the output of the PFP instruction storage logic; i.e., IR 0-15 represent a 16-bit instruction previously fetched from program memory. The IR bus IR 1-15 is fed directly to the FPU and provides the input to the floating-point instruction register. IR10 and IR11 provide conditioned inputs to the ALU control logic for determination of the carry bit in ALC operations. IR1 -IR4 provide inputs to the ACS/ACD selection logic, which determines the state of CMEM 10, 11 and CMEM 15, 16, during an instruction address generation operation.

(11) PFP Instruction Storage and Control Logic. The PFP instruction storage consists of four 16 x 4 two port RAMs, configured as a 16 x 16 dual port RAM, one set of outputs is not used. It is comprised of U65, U66, U69, and U70 on the CPU PFP PCB. The data inputs to the instruction storage elements are MEMOUT 0-15, which represent the contents of the memory out register during an instruction fetch, as determined by the memory control logic. The outputs of storage elements drive the PFP bus. This causes a 16-bit instruction to appear on the PFP bus during a read operation. The outputs are disabled when the PFP bus is being driven from ALUOUT.

The PFP instruction store is addressed by one of two minor program counters, depending on whether a read or write function is required. The counters are the current instruction counter which supplies the read address, and the write address counter which supplies the write address. PC 8-15 is an 8-bit binary counter, parallel loaded from ALUOUT, The current instruction PC is enabled for counting by INCPC and is clocked by BMEMCLK. The write address PC is enabled for counting by LOADINST and is clocked by PFPMEMCLK; it is inhibited from counting if a control memory wait condition exists.

Prefetched instructions are written into the PFP instruction array coincident with BMEMCLK when enabled by LOADINST. In semiconductor memory systems prefetching may be eight instructions ahead of the current instruction. in core memory systems prefetching may be two instructions ahead of current instructions. This procedure allows the microprogram (control memory) to function asynchronously with respect to instruction fetching, and thereby execute at greater speed. A control PROM (U67) determines how far ahead prefetching is from the current instruction. The PROM is a 512 x 4 device, with only four outputs in use. The address is formed by PFPBPC 12-15 and PC 12-15, and the contents signify the state of prefetching in terms of the difference between two counters, as follows:

- FULL = Stop prefetching, eight or two instructions as the case may be, have been prefetched.
- CTG1 = Prefetching is more than one instruction ahead of the current instruction.

- CTEQ1 = Prefetching is one ahead of the current instruction.
- CTEQ0 = Prefetching is equal to the current instruction.

The FULL signal stops prefetching. The remaining three signals provide conditional inputs to the RFP ready logic, in preparation for the initiation of a prefetch cycle.

A third counter is used in the PFP to limit access in the current block of 128 words. The counter consists of two 4-bit binary counters (U59 and U60) on CPU PFP PCB configured as an 8-bit counter. The counter is loaded from at the same time as the current Instruction PC and the write address PC. The counter is clocked by BMEMCLK and enabled for counting, incrementing the counter at the beginning of each prefetch cycle. When the counter reaches 128 (127 octal), regardless of the value previously loaded, the end of Current Block condition is activated. When the counter is preloaded, EOCB activates preventing initiation of a prefetch cycle. This means that the prefetch operation has exhausted the current block, not that all of the prefetched instructions have been executed. Consequently, a PFP ready state can still exist until all of the current instructions have been executed at which time the MAP logic will direct the microprogram to another memory block, or, until a jump instruction is executed at which time the counters will be reloaded and the end of block condition will no longer exist.

(12) Console PROM. The console PROM consists of two 2k x 8 PROM chips, configured as a 2k x 16 PROM (U I and U2 on the CPU PFP PCB). The PROM is enabled by CONROMSRCENB from the R1 decode of lesser random field 1 (RAND1). The PROM address is specified by ALUOUT5-ALUOUTI 5 and the PROM outputs are directly connected to ALUIN0-15.

(13) Control Memory (Microcode Storage). The control memory is located on the CPU PROM PCB. It consists of sixteen 2k x 8 PROMS, configured as a 4k x 64 memory system. Control memory is functionally divided into two 2k x 64 banks, bank A and bank A, as shown. The bank is selected by CMEMADRA, which IS derived from CMEM 57 (control memory expansion bit). When CMEMADRA is low bank A is selected, and when high ban A is selected. The individual location, within the selected bank is addressed by CMEMADRO-10 (11 bits corresponding to an address range of 0-3777 octal), to provide selection of one location with 2048 (2k).

(14) Control Memory Address. The control memory address CMEMADRA, 0-10 (12 bits) is derived from one of four sources as follows:

- Start address generator (SAGE)
- Instruction decode logic (partial decode)
- Microsequencer
- The address field of the microinstruction

(15) Start Address Generator. The SAGE consists of the priority arbitration logic, and associated address generation logic. The logic elements are installed on the CPU PROM PCB.

Priority is assigned to requests in the following order:

- Data channel
- Non-maskable interrupt or 1/0
- Prefetch processor
- Instruction

The gating input to the priority logic is USEQ3, which is generated by the micro-sequencer. It signifies that a start address should be generated. The priority logic shows that if no other requests are active INSTSAGE is the buffered output of USEQ3. The starting address is derived from U18 and U19. Only U18 is enabled during an instruction SAGE and that only U19 is enabled in the other cases.

(16) Decode Address Logic (Processors 1,1X,2,2X). The decode address logic. It generates an address during microsequence 2, according to whether there is a data channel decode (DCHDECODE) or not (NONDCHDECODE). The source of the decoded address is determined by the type of instruction appearing on the PFP bus. I/O instructions are identified when NORMAL I/O DECODE is low. The decoded address is read from U59, a 512 X 8 PROM, according to the logic state of the instruction bits.

Special I/O instructions, which are usually floating-point instructions, are identified when SPEC I/O 1 + 2 is low. The decoded address is read from U41, a 512 x 8 PROM, according to the logic state of the instruction bits. The instruction bits are derived partly from the multiplexer U43.

A file is maintained for each possible user. The file is addressed by five of the most significant six bits of the machine-generated 15-bit address, called logical address. The file contains 10 address bits, which are appended to the most significant end of the least significant 10 bits of the logical address. This forms a 20-bit physical address. In this way using a logical address space to assembled 1 k-word pages from anywhere in memory arranges the files as a supervisory program. Figure 1-13 summarizes the procedure.

Memory protection prevents one user from accessing another user's memory space. If one user does not require its full logical address space, the unused memory may be allocated to another user. The unused logical pages of the first user are declared invalid to that user. Should the first user then reference those pages, a validity protection trap sequence ensues. Pages of user logical address space may be write-protected to prevent modification of stored data. I/O may be protected from user use to prevent DMA cycles to other user address spaces.

The MAP logic is contained on the CPU MAP PCB and also includes the various address and data buffers that interface to the memory in bus.

(17) MAP File (Processors 1,1X,2,2X). The MAP file consists of a 1k x 16 bit RAM. It is configured from sixteen 1k x 1 bit RAM elements. The data inputs are derived from the 16-bit PFP bus. Functionally, the RAM is divided into two halves; one half contains the MAP files and the other half is not used.

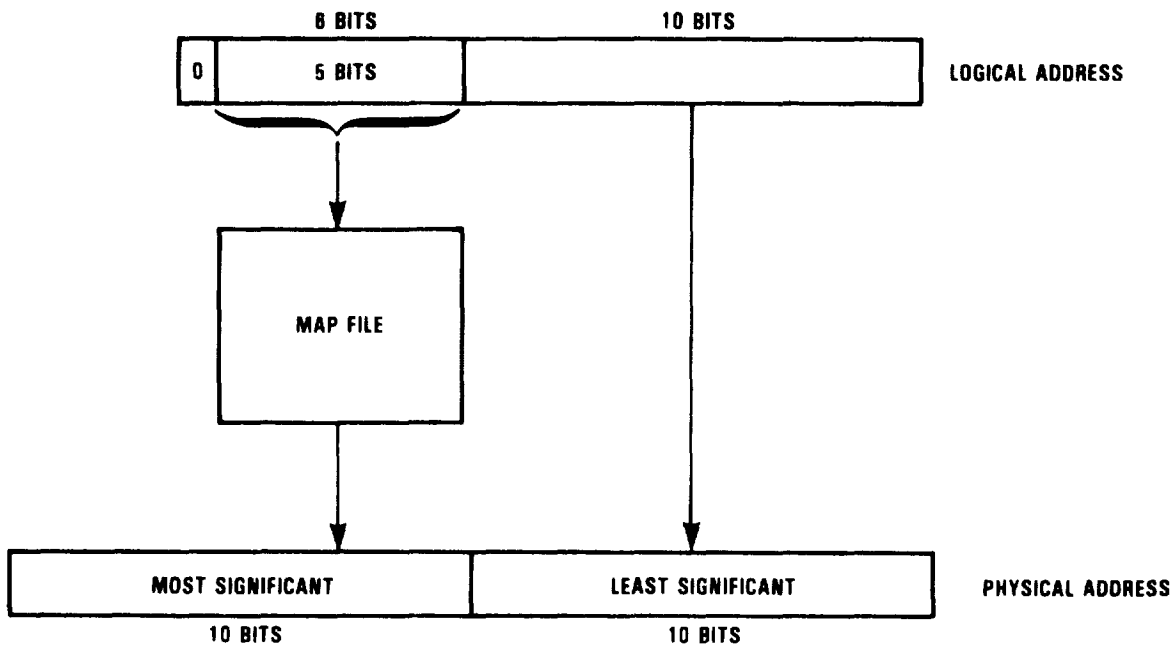

Figure 1-13. Memory Allocation (Physical Address)

Of the 512 locations assigned to the MAP files, only half are used (256 locations), which permits eight files of 32 locations each.

The file addressing structure consists of 10 bits, MAO-MA3 being most significant and MAPADRA, 1-5 being least significant. MAPADRA is always low (zero) and MAPADR1-5 are derived from ALUOUTI-5. The MAP file is accessed for write (input) operations and for read (output) operations.

The outputs MAPOUT0-5, MEMININ0-5, and MEMININ16-19, represent the 10 most significant bits of a physical memory address, plus its protection bits (MAPOUT0-5). The inputs PFP0-15 represent the corresponding information when loading the MAP files.

(18) MAP File and Scratchpad Memory (Processor 3,3X,4,4X). The MAP file and scratchpad memory consists of a 1 k x 16 bit RAM. It is configured from sixteen 1k x 1 bit RAM elements. The data inputs are derived from the 16-bit PFP bus. Functionally, the RAM is divided into two halves, one half containing the MAP files and the other half containing the scratchpad memory.

The scratchpad memory contains the virtual console internal registers and the optional floating-point instruction set (FPIS). Unassigned locations are used for scratch-pad purposes. Of the 512 locations assigned to the MAP files only half are used (256 locations), which permits a maximum of eight files, each with 32 locations. The MAP file or scratchpad is accessed for write (input) operations and for read (Output) operations.

The outputs MAPOUT0-5, MEMININ0-5, and MEMININ16-19, may represent the 16-bit content of an internal register, when the CPU is in VC mode; a 16-bit floating-point instruction, when the firmware supported FPIS is specified, the 10 most significant bits of a physical memory address, plus its protection bits (MAPOUT0-5), when reading the MAP file. It follows that the inputs may represent any of the foregoing, when loading or modifying an internal register, when loading FPIS registers, when loading the MAP files, and when manipulating data.

(19) PFP Program Counter (PFPPC). The PFP program counter consists of two register U54 and U64, and two 4-bit counters (U41-U31), configured as a 7-bit counter. The counter is parallel loaded from the MAP file address outputs and ALUOUT6-15. The counting element (U41, U31) is incremented each time a fetch cycle is started, since it is only seven bits long it may specify only one address within a 128 word block. The counter outputs provide a 20-bit physical address to memory during an instruction fetch cycle.

(20) CPU Mapped Address. The CPU must have the capability to provide a 20-bit physical address to memory during the initiation of a memory reference operation, as opposed to an instruction fetch. During the initial sequence of the memory reference the assembled 20-bit physical address will be gated onto the MEMIN bus in significant order.

(21) CPU Logical Addressing (Non-mapped). In the case of logical or non-mapped addressing, the ALU provides a 15-bit address. When the memory reference cycle is initiated (read or write), a 16-bit address appears derived from the ALU.

(22) CPU Write Data. Write data is placed on the MEMIN bus immediately after a 20-bit physical address or a 15-bit logical address. The 16 data bits are derived from the ALU outputs.

(23) Write Current Block Detector. The WCB detector consists of two 12-bit comparators, configured as two 8-bit comparators, which functionally act as a single 16-bit comparator (i.e., two sets of 16-bit inputs). The comparison is made between the address in the PC and the address on the MEMIN bus during a memory write cycle. The four least significant bits of PC and MEMIN are not compared. The next three least significant inputs to the comparator are grounded so that the comparison is made within a 128 address block.

When a comparison occurs the WCB flip-flop clock to set. This indicates to the CPU that an attempt has been made to write into an area in memory while prefetching is in progress, The microcode restarts the prefetcher causing the WCB flip-flop to reset at the next BMEMCLK.

(24) MAP Exception and Data Channel Violation. Exceptions and violations are caused by attempted accesses to memory outside a user's space, by a write to a write protected block, by a write to a validity protected block, or by starting the PFP in a block outside the user's space. If any of the foregoing conditions occur the MAP exception flip-flop or the data channel violation flip-flop is clocked into the set state.

(25) MAP Control Field Register (Processors 1,1X,2,2X). The MAP control field register consists of two octal decoders U102, U87, and two octal 8-bit registers U95, U85. The octal decoders decode the MAP control field of the microinstruction (CMEM59, 60, 61) according to the logic state of CMEM 58. The decoders are latched into the registers.

(26) MAP Control Field Register (Processors 3,3X,4,4X). The MAP control field register consists of two 8-bit registers U95, U85, and two octal decoders U 102, U87. The octal decoders decode the MAP control field of the microinstruction according to the logic state of CMEM 58. The processor uses four of the decodes, Read MAP (RDMAP), write MAP (WTMAP), clear program exception (CLRPMS), and load display (LDDSPLY). The load display control signal enables the bite display to be driven indicating the self-test fault code.

(27) MAP Status Register (MSR). The MAP status register is internal to the ALU. The microcode updates the MSR prior to, and following all mapped memory access operations.

(28) MAP Violation Register (Processors 1,1X,2,2X). The MAP violation register (MVR) outputs are gated onto ALUIN. When a violation occurs, the detection logic activates, and the CPU is accordingly notified.

(29) MAP Control Logic (Processors 1,1X,2,2X). The MAP control logic consists of four flip-flops. U44 is controlled by the set and reset inputs and is not clocked; i.e., controlled by the microcode. The first half of U27 is the single instruction cycle (SIC) flip-flop, the other half is the single data cycle (SDC) flip-flop, corresponding to the user instruction MAP and data MAP respectively. The first half of U44 is the PCDATA flip-flop and the other half is the DATA flip-flop, corresponding to an instruction cycle and a memory reference cycle.

(30) MAP File Address Control Logic (Processors 1,1X,2,2X). This logic generates the MAP file address. If a data channel cycle is in progress the address bits are derived from U25 and will normally be all zero bits. Otherwise the address bits are derived from U37.

(31) MAP File Adddress Control Logic (Processors 3,3X,4,4X). This logic generates the MAP file address. If a data channel cycle is in progress the file address bits are derived from U25.

(32) I/O Protect File (Processors 1,1X,2,2X). The I/O protect file consists of a 1k x 1 bit RAM (U20) and the address multiplexer U30 and U10 . The file corresponds to 16 maps, each map containing 64 bits, which relate to a maximum of 64 I/O devices. Only eight of the MAPS are used, as is the case in the MAP file. For a given I/O adddress, the file determines whether or not the user is authorized to use that device. A one bit signifies that the device is protected from use by that particular user. A zero bit signifies that the user is authorized to use the device. Refer to appendix C, D, and E for additional I/O information.

The CPU accesses the file to write the protect bits in the respective protect files. The file address (10 bits) is made up from the MAP file address bits (MAO-MA3), together with six of the outputs from the address multiplexer. When an I/O operation is started the address multiplexer select the device address code to supplement the MAP file address bits. If I/O protection is in force an I/O fault is signified.

(33) Last Address File (Processors 1,1X,2,2X). The last address file consists of two 8-bit buffer registers, U48 and U38, of which only six bit positions are used, and three 8-bit shift registers U18, U84, and U28. The shift registers are connected in series and the serial output is gated onto ALU IN.

Buffer register U48 is parallel loaded from MAPADRA, 1-5 by PC CLK and register U38 is likewise loaded by BMEMCLK. The outputs of both registers are connected, so that only one of the register's outputs are used, depending on whether the current memory reference is an instruction cycle or a data cycle. The individual shift registers are parallel loaded simultaneously, A shift and load operation cannot be coincident. In effect, the shift register contains the least significant 10 physical address bits, ail of which point to a 20-bit physical address. The additional information supplied denotes whether or not a data channel cycle was in progress, whether or not the CPU was in Executive mode, and whether or not a nuclear event took place. As the information is shifted out of the shift register (file), one bits are shifted in.

1-17. FLOATING POINT UNIT (FPU) DESCRIPTION

The floating point unit consists of three boards: FPU-A, FPU-B, and the FPU-C66 for processors 1,1X,2,2X or the FPU-CE for processors 3,3X,4,4X. The FPU-A board contains the exponent loop and part of the mantissa loop. The FPU-B board contains the remaining part of the mantissa loop. The FPU-C66 and FPU-CE boards contain the control and timing logic, including the FP microcontroller, installation register, microcode storage logic, and microinstruction decode logic. The paragraphs to follow provide general information with respect to the CPU-FPU interface and handshaking protocol, number representation, and brief descriptions of the various algorithms used to compute the results.

a. CPU-FPU Interface. The CPU-FPU interface is represented in block diagram form in figure 1-14. The CPU initiates the operation of the FPU and controls all data transfers between itself and the FPU, and between the FPU and memory. In all other respects the FPU functions independently.

The CPU transfers numerical data to the FPU on the MEMIN bus. The FPU places information on MEMIN for transfer to memory, under the control of the CPU. The FPU is notified of all memory transfers from the CPU. Numerical data is also transferred from memory to the FPU on MEMOUT, again under control of the CPU.

Floating-point instructions are transferred from the CPU to the FPU (the FPU uses only nine instruction bits) on an extension of the CPU IR. The CPU notifies the FPU that the instruction is available. Information from the FPU to the CPU is transferred on MEMOUT. The information may be the FPU status, or the result of a floating-point computation. A computation may be aborted at any time by the CPU.

The CPU monitors signals from the FPU before issuing an instruction, or initiating a memory transfer from FPU-memory, or from memory-FPU. The CPU is notified that the FPU is either busy executing a previous instruction, or that a trap condition has occurred. The FPU will not accept an instruction from the CPU if it is executing a previous instruction, or a trap condition exists.

The CPU enables the FPU to recognize that a valid transfer of information is taking place. The CPU also notifies the CPU that the skip instruction test was successfully executed. The FPU notifies the CPU that data requiring formatting is ready for transfer.

b Number Representation. The FPU operates on single-precision, extended-precision, or double-precision numbers. Single-precision numbers consist of four bytes of numerical data, extended-precision numbers consist of six bytes of numerical data, and double--precision numbers consist of eight bytes of numerical data. In all cases, the first byte is a single sign bit (0^5positive, 1^5negative). The remaining seven bits constitute the exponent value of the number. All remaining bytes contain the mantissa or fractional part of the number.

The value of a floating-point number is represented as 16E x m, where E is the exponent and m is the mantissa. The mantissa is always a positive fraction. The binary radix point, corresponding to the decimal point, is imagined to be between bits 7 and 8 of the number. Thus, bit 8 represents the value 1/2, bit 9 the value 1/4, bit 10 the value 1/8, and so on.

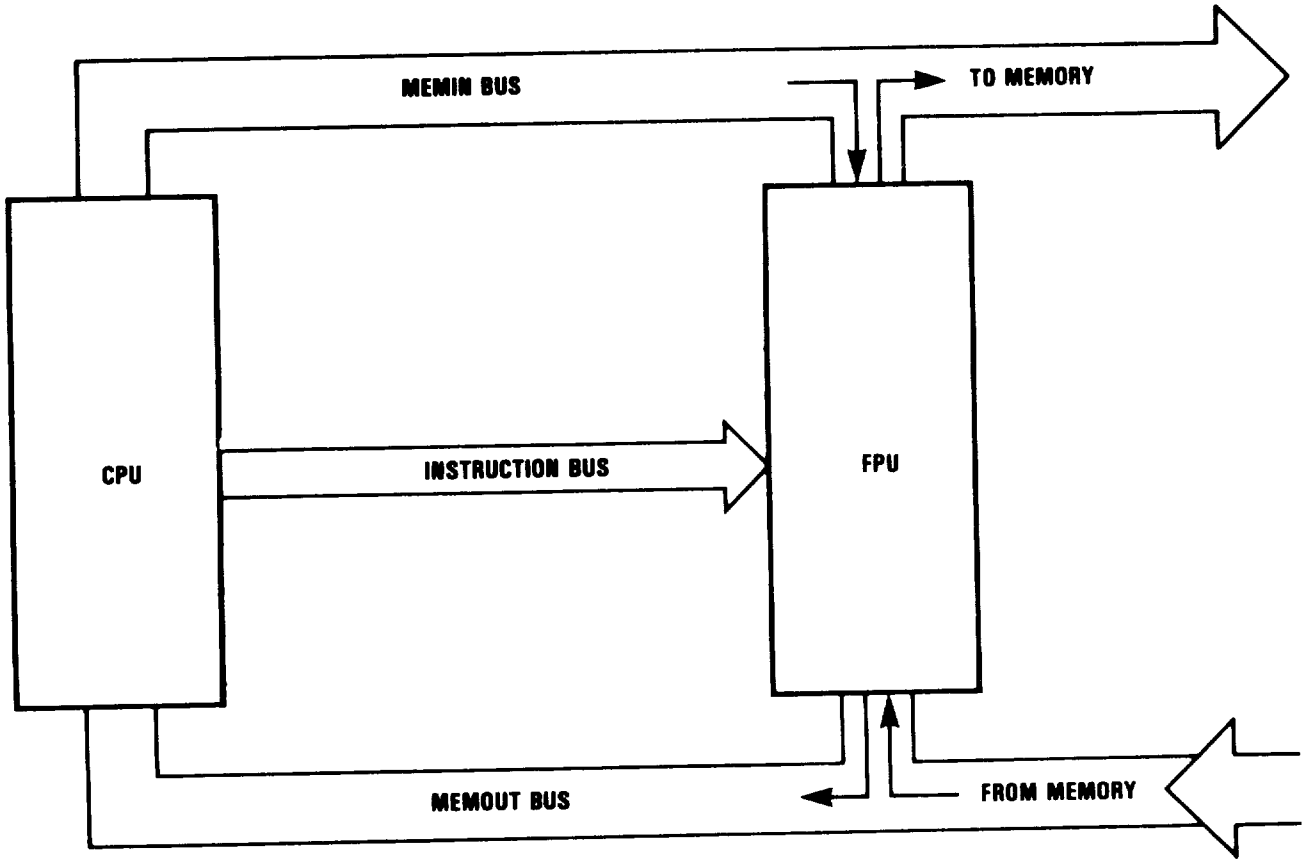

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Figure 1-14. CPU-FPU Interface, Simplified Block Diagram

The most significant bit of the first word is the sign of the complete number. The next seven bits are the exponent and the most significant bit of the exponent is its sign bit. To maximize the range of the exponent in both the positive and negative direction an excess 6410 code is used.

(1) Number Representations in Processors 1, 1X, 2, 2X. In the V1, V1X, V2 and V2X versions increasing or decreasing the exponent by one, is equivalent to multiplying or dividing the mantissa by 16 respectively. This is equivalent to shifting the mantissa left or right four bit positions (one hex digit).

To avoid the problem of losing significance during floating-point operations, the mantissa is maintained as a fraction equal to, or greater than 1/16 but less than one, by the process of normalization. Normalization shifts the mantissa left one hex digit at a time until the high order four bits of the mantissa signify a non-zero quantity. For every hexadecimal digit left shifted, the exponent value is decreased by one. It is possible for the three high order bits of a normalized mantissa to be zero (0001).

Zero is represented by a floating-point number having all zero bits, including sign and exponent, in single-, extended-, and double-precision operations, and is known as “true zero”. When a calculation results in a zero mantissa, the FPU converts the complete number to a true zero automatically. True zero is a positive number. A negative zero is not possible as the result of a calculation. The manipulation of floating point numbers by the FPU is carried out in terms of hex digits (four bits at a time).

(2) Number Representation in the Processors 3, 3X, 4, 4X. The exponent sign bit generated by excess 64 code is the complement of the actual sign in versions 3, 3X, 4 and 4X. Increasing or decreasing the exponent by one is equivalent to multiplying or dividing the mantissa by 16 respectively. This is equivalent to shifting the mantissa left or right four bit positions (one hex digit).

To avoid the problem of losing significance during floating-point operations, the mantissa is maintained as a fraction equal to or greater than 1/16 but less than one, by the process of normalization. Normalization shifts the mantissa left one hex digit at a time until the high order four bits of the mantissa signify a non-zero quantity. For every hexadecimal digit left shifted, the exponent value is decreased by one. It is possible for the three high-order bits of a normalized mantissa to be zero (0001).

Zero is represented by a floating-point number having all zero bits, including sign and exponent, in single-, extended-, and double-precision operations, and is known as “true zero”. When a calculation results in a zero mantissa, the FPU converts the comp!ete number to a true zero automatically. True zero is a positive number. A negative zero is not possible as the result of a calculation. The manipulation of floating-point numbers by the FPU is carried out in terms of hex digits (four bits at a time).

c. Floating-Point Computations. The following paragraphs briefly describe how the FPU performs-various arithmetic operations. The floating-point numbers (operands) are derived from main memory or from four floating-point accumulators in the FPU. Results are stored either in main memory, or the accumulators; or they are transferred to the CPU.

(1) Floating-Point Multiply. The exponents of the two numbers are added together and the mantissas of the two numbers are multiplied. When the exponents are added, 64 is subtracted from the intermediate result to maintain excess 64 notation. If the exponent processing produces either overflow or underflow, it is held off until normalization, since normalization may correct the condition. If normalization does not correct the condition, the corresponding flag in the status register is set. The number will be correct except that, for exponent overflow the exponent is 128 too small and for underflow is 128 too large.

Before entering the mantissa multiply loop, the FPU microprogram stores multiples of the multiplicand in four firmware scratchpad registers. The multiples are 8, 4, 2, 1 respectively, which when added together constitute 15 times the multiples and any combination from 1 to 15 can be obtained.

The microprogram examines each hex digit in the multiplier, starting with the least significant, then makes a partial result from adding multiples together. The multiplier is shifted right to examine the next hex digit and the partial result is shifted left, the addition of the previous partial result to the specified number of multiples produces the next partial result. A counter keeps in step with the number of iterations. When the counter has counted down to zero, the intermediate or unnormalized result is available.

There is one restriction in the multiply loop; it is, that only two multiples can be added during one pass. Suppose the multiplier digit was 7 hex. This would require the additions of the multiples 4 + 2 + 1, but only the 4 + 2, or 2 + 1 addition could take place at one time. In this case and several others a subtraction, not an addition, takes place; i.e., 8 minus 1, and that result is added to the previous partial result. The intermediate result is finally normalized and an overflow or underflow condition is flagged in the status register. The signs are added algebraically.

(2) Floating-Point Divide. The exponent of the divisor is subtracted from the exponent of the dividend. The dividend mantissa is divided by the divisor mantissa. When exponents are subtracted, 64 is added to the result to maintain excess 64 notation. The result becomes the exponent of the intermediate result. The sign of the intermediate result is determined by algebraic rules. If exponent processing produces either overflow or underflow, the corresponding bit in the status register is set. The number is correct, except that for exponent overflow the exponent is 128 too small and for underflow the exponent is 128 too large.

The mantissa of the divisor is checked for zero. If the mantissa is zero, the division zero (DVZ) flag in the status register is set and the operation is terminated. If the mantissa of the divisor is non-zero the divide algorithm begins.

The two mantissas are compared. If the dividend mantissa is larger than or equal to the divisor mantissa, the dividend mantissa is shifted one hex digit and the intermediate exponent is increased by one. The mantissas are then divided by a series of right shifts and subtractions to produce partial results. Such iterations are counted. When the count reaches zero, the last partial result becomes the quotient of the intermediate result. Since the operands are assumed to be normalized, and because division with such operands produces a normalized result, no normalization of the result takes place.

(3) Floating-Point Addition. Floating-point addition consists of an exponent comparison and a mantissa addition. The exponents of the two numbers are compared. The mantissa of the number with the smaller exponent is shifted right. This alignment of the mantissa is accomplished by taking the absolute value of the difference between the two exponents and shifting the mantissa with the lower exponent to the right of that number of hex digits, A guard digit is provided to mark the boundary so that all four bits shifted out from the right end of the mantissa are lost. If all significant digits are shifted out of the mantissa, the addition is equivalent to adding zero to the number with the larger exponent. In double precision this requires a shift of at least 15 hex digits, in extended precision a shift of 11 hex digits. In single precision, a shift of 7 hex digits.

Following alinement, the two mantissas are added. The sum provides the intermediate result and includes a guard digit, which is used if normalization is required. The sign of the intermediate result is determined from the signs of two operands by the rules of algebra. When the mantissa addition produces a carry out of the high order end, the mantissa in the intermediate result is shifted right one hex digit and the exponent is incremented by one. If this produces an exponent overflow, the associated bit in the status register is set, The sum is correct, except that the exponent is 128 too small. When there is no mantissa overflow, the mantissa of the intermediate result is examined for leading zeros. If the mantissa is all zeros, a true zero is placed in the result and the operation terminates. If the mantissa is non-zero, the intermediate result is normalized. If normalization results in an exponent underflow, the associated bit in the status register is set. The sum is correct, except that the exponent is 128 too large.

(4) Floating-Point Subtraction. The sign of the floating-point number representing the subtrahend is inverted and that number is added to the floating-point number representing the minuend. Following the sign inversion, the operation is equivalent to floating-point addition.

(5) Floating-Point Halve. The halve operation effectively divides a floating-point number by two. The mantissa of the number is shifted right one bit position (not one hex digit position). The vacated bit position is filled with a zero bit. The bit shifted out moves into the guard digit. The number is then normalized. If normalization causes an exponent underflow, the associated bit in the status register is set. The number is correct, except that the exponent is 128 too large.

(6) Floating-Point Integerize. Makes a whole number from a compound number containing a fraction. The fractional portion of the number (if any) is zeroed, and the number is then normalized. If the absolute value of the number is less than one, the result is true zero.

(7) Floating-Point Scale. Shifts the mantissa of the floating-point number either right or left, according to the scale factor bits 1-7. The scale factor is stored in Accumulator O prior to the operation and floating-point number and temporarily stored in another accumulator (FPAC). Bits 1-7 of the scale factor are treated as an exponent in Excess 64 notation. The difference between this exponent and the exponent in FPAC is computed by subtracting the exponent in FPAC from AC0 bits 1-7. If the difference is zero the operation is terminated. If the difference is positive the mantissa in FPAC is shifted right that number

of hex digits. If the difference is negative, the mantissa is left shifted that number of digits. After the shift operation, ACO bits 1-7 replace the exponent contained in FPAC. Bits shifted out of either end of the mantissa are lost. If the entire mantissa is shifted out FPAC is set to true zero.

(8) Floating-Point Negate. Inverts the sign bit of the floating-point number. The remaining bits of the number remain unchanged. If the number is true zero the sign bit is not changed. If the mantissa is zero, the sign and exponent are set to zero.

d. Floating-Point Microcontroller. The microcontroller consists of an instruction register; control storage address generation logic, including a sequencer and its control logic; 512 words of control storage for 72-bit microinstruction; a microinstruction register, including decode logic; a floating-point status register; memory bus interface logic, including data registers.

e. Floating-Point Instruction Register. The instruction register consists of two 8-bit latches, The inputs are derived from the CPU instruction register outputs and are latched when FPI goes high. When the CPU sends a floating-point instruction to the FPU across the instruction register bus, it activates FPINST. If the FPU is not busy; i.e., is not executing a previous instruction, then FPINST activates FPI and the instruction is latched. The FPU utilizes nine instruction bits FIR1-9, which initially provide the starting address to the control store addressing logic.

f. Control Store (Microinstruction Storage). The control store consists of nine 512 x 8-bit PROMS, configured as a single storage element containing 512 microinstruction, each microinstruction being 72 bits wide. The control storage address (microinstruction location) is specified by the nine address bits CA0-8. Eight of the PROMS are permanently enabled. The ninth PROM is disabled if a Restart operation occurs. No test is made to determine control sequencing during a restart.

g. Control Store Address Generation. The control store address bits are derived from one of four sources; namely, the start address, the vector or random address, the jump address field of the microinstruction, and the microsequencer. The course is determined by the microsequencer control bits, which are derived from one or the other of the microinstruction sequence fields based on whether or not the tested condition was true or false.

h. Floating-Point Status Register (FPSR). The FPSR consists of two quad J-K registers and a 4-bit counter. The counter is not enabled for counting, but can be enabled for parallel loading from the two outputs, which selects the zero (Z) and negative (N) bits from one of four sources.

i. Memory Bus Interface. Internal bus (MEM0-15) interfaces with both the principal memory buses, depending on the direction of data or information transfer.

NOTE

MEMIN and MEMOUT are unidirectional buses; i.e., data flow is always in the same direction.

The IN and OUT control signals are determined by the decodes of random operation field 4 of the microinstruction. IN controls the transfer of numerical data and status information from the CPU to the FPU. OUT controls the transfer of numerical data from memory to the FPU.

j. EPU Clock Generation. The clock rate is determined by CB37 and CB38, the two most significant bits of the microinstruction clock rate field. The FPU clock rate is 5.0 MHz; the clock period is 200 nS, including register clock (RCLK). The output of U7 is a 10 MHz clock with a 250/. duty cycle, and provides the toggle inputs to both halves of U47. The two flip-flops toggle synchronously.

One half of U64 is toggled at a 5.0 MHz rate from the output of U47 (Q). Its output is a 2.5 MHz square wave (400 nS period). The inverse of this output from U73 is ORed with the output of U47 (Q) to provide 2.5 MHz clocks with a 75% duty cycle. RCLK is also at the same rate and duty cycle in this case.

k. I/O Timing Logic. The FPU input/output timing diagram is given in figure 1-15, and shows the timing relationship for each of the four types of data transfer. Refer to appendix D for additional I/O information.

Data transfers between the FPU and memory occur during the data phase of a memory write or read operation. The CPU initiates the data transfer in the same way it starts any memory operation by driving MEMSTART low. It notifies the FPU of the transfer by activating FPUMEM. The CPU sends the address to memory (MEMIN) during the address phase of the memory operation. During the data phase the FPU either sends a data word to memory (DRIVEA), or receives data from memory (OUT).

Data transfers between the CPU and FPU take place during the data phase of a dummy memory operation. When the CPU initiates the operation, it inhibits memory by activating INHSEL, still activates MEMSTART but does not activate FPUMEM. The FPU is notified of transfer when the CPU activates FPCPU. In this case the control signals are IN (CPU to FPU) and DRIVEB (FPU TO CPU). Note that the gating signal VALIDFPCPU cannot be activated during memory read or write operations.

The pause flip-flop is clocked set during all FPU I/O cycles (IOCYC = low), providing a restart condition has not occurred (DRESTRT = low). PAUSE prevents the generation of FPU clock during the pause period, in order to synchronize the transfer of valid data to or from the memory buses. Note that for all data transfers the clock rate is 200 nS and that neither CB37 nor CB38 should be high.

The principal timing element is a 4-bit dual output register, which functions as a 3-bit shifter and single-bit latch in core memory systems, and as a 4-bit shifter in semiconductor memory systems. In the latter case CMEMWAIT will always be high. The effective serial input **to** the shifter will be a one bit during the data phase of a memory write operation and the drive A flip-flop will be clocked set on the next occurrence of BMEMCLK. The input to the single-bit latch (4D) will be low during the data phase of a memory write operation, and will be held low if a memory wait condition exists (core memory).

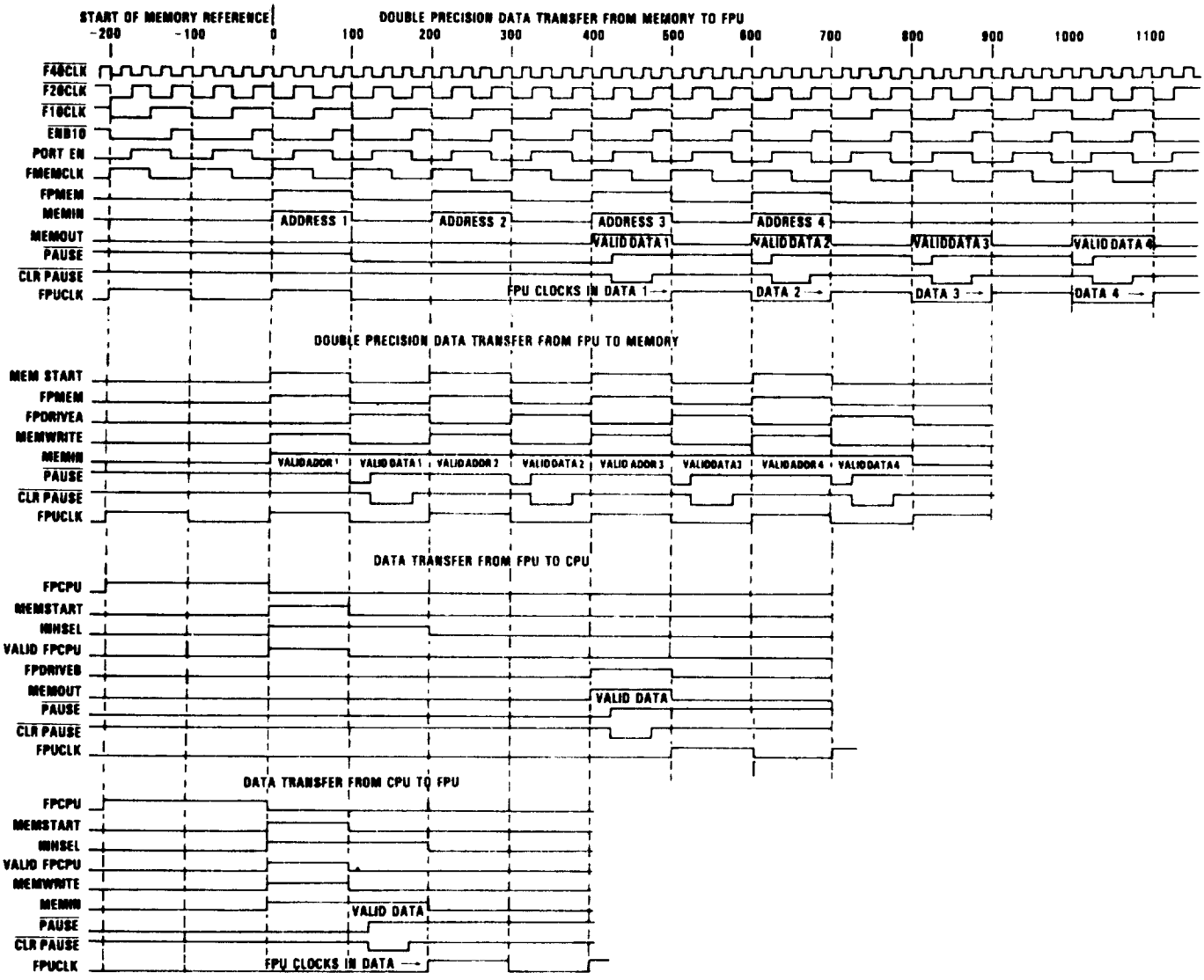

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Figure 1-15. I/O Timing (FPU)

During a memory read operation (memory to FPU) neither APEN or BPEN will be active, in which case the serial input to the shifter will be a zero bit and the input to the single-bit latch will be a one bit; this is also true for a CPU to FPU data transfer. During an FPU to CPU data transfer BPEN will be activated. The serial input to the shifter will be zero and the input to the single-bit latch will be a one bit.

When the single-bit latch is set, the pause flip-flop is cleared coincident with the next PORTEN and BMEMCLK clock pulse; however if a memory wait condition exists the Pause flip-flop will not be cleared. The function of the shifter is to ensure the correct timing relationship for data transfers.

l. **Exponent Processing Loop.** The exponent processing logic is contained on the FPU-A board. The loop is eight bits wide and consists of the following functional components:

- Two files (RAMs)
- Two working registers, A and B, identified by the microcode as the exponent A register (EAR) and the exponent B register (EBR) (EAR) and (EBR)
- An ALU
- A 2-1 multiplexer
- A 4-1 multiplexer

m. **Mantissa Processing Loop.** The mantissa processing logic is contained on the FPU-A board and FPU-B board. The mantissa loop is 64 bits wide in order to accommodate double precision numbers. FPU-A manipulates the high order 28 bits and FPU-B manipulates the remaining 36 bits.

- A file (RAMs), FPU-A elements, and FPU-B elements
- A 2-1 multiplexer, FPU-A, and FPU-B
- An ALU, FPU-A, and FPU-B
- MPR working register, FPU-A, and FPU-B
- MQR working register, FPU-A, and FPU-B
- A Pass-1 left multiplexer, FPU-A, and FPU-B
- A 16 left-4 right multiplexer, FPU-A, and FPU-B
- A barrel shifter, FPU-A, and FPU-B

1-11. CORE MEMORY DESCRIPTION

A core memory system consists of a single memory controller board and up to 32 memory modules. The controller controls both internal memory and external memory, with respect to the processor chassis. A core memory module consists of three PCBS: an X-driver, a Y-driver, and a 32k word stack. Up to 1024k words (1 M) may be accommodated, in increments of 32k words. The minimum hardware configuration is one 32k word module, which is installed in the processor chassis together with the controller. An additional 32k word module may be

installed in the processor chassis, making a total of 64k words of internal memory. Any further 32k word increments require the addition of one or more remote memory chassis (RMC) to the system. Each RMC added to the system can accommodate six memory modules (192k words) allowing up to five RMCS to be installed.

a. Core Memory Controller Model 1755. The controller performs six functions, as follows:

- Memory enable control
- Internal core memory control
- Remote core memory control
- Parity generation/checking
- Interrupt control
- System clock generation

The following paragraphs describe each of the functions performed by the controller and the respective timing relationships.

(1) Memory Enable Control. The functions of the memory enable control logic are to determine whether or not a memory reference is being made; the type of reference (read or write); whether internal or remote memory is being referenced, and whether or not the memory is busy processing a previous reference. It also generates the appropriate address and data strobes as applicable, by monitoring the MEMSTART and MEMWRITE signals.

(2) Internal Memory Control. The internal memory control logic generates specific timing pulses to the internal core memory modules, following initiation by the memory enable control logic. It also generates status signals to signify when read data is available and when the memory reference has been completed.

(3) Remote Memory Control. The remote memory control logic provides the interface control for the remote memory bus. It generates the timing sequence for bus transfers, and also generates control signals that signify when the memory reference has been completed and, as applicable, when read data is available.

(4) Parity Generation/Checking. Odd parity is generated on a word basis, which means that 17 bits are written into memory and 17 bits are read from memory.

(5) Interrupt Control Logic. The interrupt control detects a parity error either from internal or remote memory and a remote memory power fail condition.

(6) System Clock Generation. The clock generation timing sequence is given in figure 1-16. The clock trains are distributed throughout the processor chassis.

The fundamental clock frequency is derived from a 40 MHz crystal controlled oscillator. The oscillator provides the B40 CLK output, which simultaneously clocks the timing flip-flops U71 and one half of U62. Both halves of U71 toggle on the occurrence of clock, noting that the

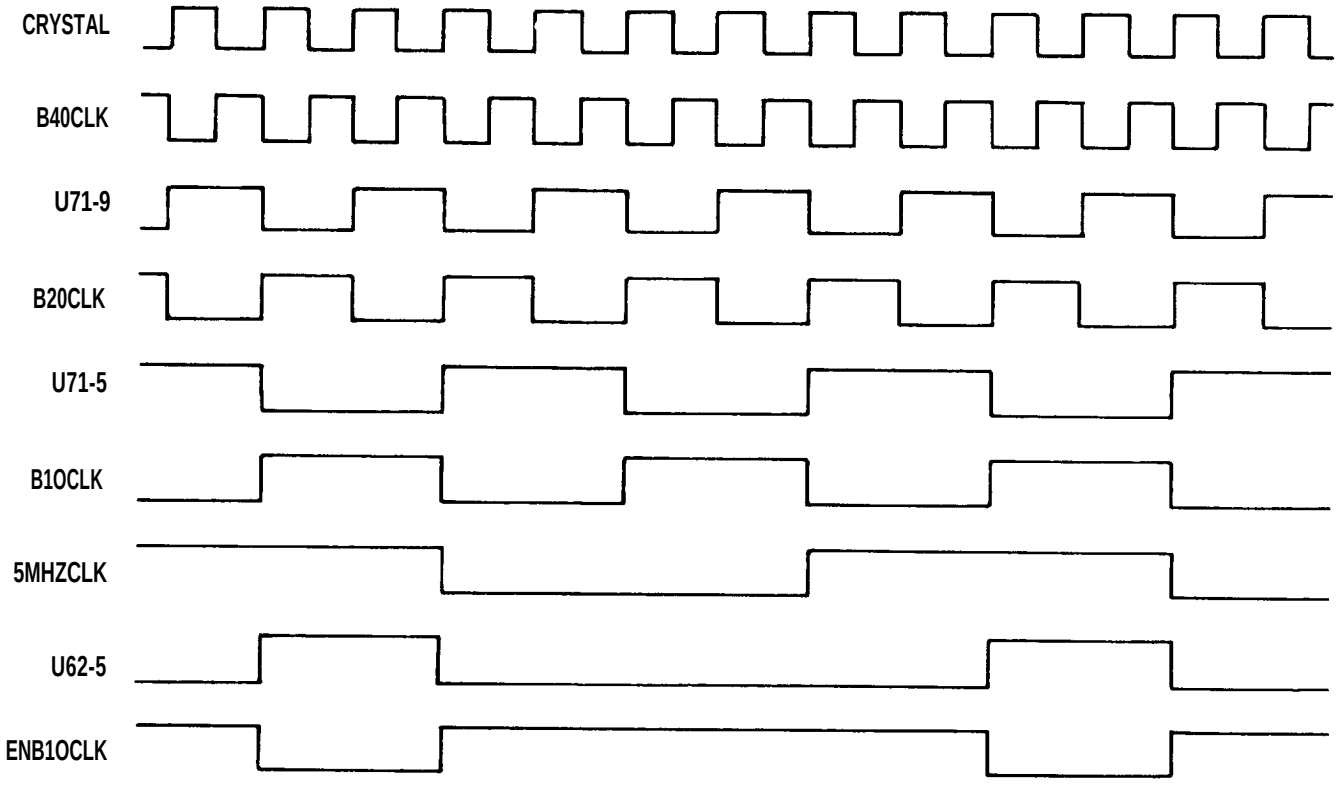

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Figure 1-16. System Clock Generation

second half of U71 derives its toggle input from the Q output of the first half of U71. The first half of U62(5 MHz clock generator) receives its clock input from the Q output of the second half of U71. The second half of U62 toggles twice while the second half of U71 is in the reset state.

b. 32k Word Core Memory Module. The model 2019 core memory module is a 3-D, 3-wire coincident core memory packaged in a 32k x 17-bit module. Sixteen bits are used to store data and the 17th bit is an odd parity bit. Each module consists of two drive-data circuit PCBs and a stack PCB. Nominal cycle times are 1.0 us for read-restore and clear-write cycles and 1.25 us for read-modify-write cycles. Timing signals are provided by the memory controller, which interfaces with the CPU. Supply voltages of 5V, + 12V, and 15V are required. All three PCBs must be replaced if a fault condition is indicated. The PCBs are matched at the factory; any intermixing of the PCBs may seriously degrade performance.

(1) General Information. Core memories utilize the remnant property of nonlinear magnetic materials; i.e., if the saturation flux density (Bs) is produced in a ferrite core by an applied field, the residual flux density (Br) after the field is removed will be only slightly below saturation level. Binary information is stored by driving a core to positive or negative saturation (a residual flux density of +Br is defined as a binary zero, -Br as a one). Information is received from a core by driving it toward +Bs and observing the voltage across a winding threading the core. A core in the stored-zero state undergoes only a slight change in flux density (Bs - Br) and induces a very small voltage in the output winding, while a core in the stored-one state has a much larger flux-density change (Bs + Br) and a correspondingly larger induced output voltage. Since interrogating a core places it in the stored-zero state, each read operation must be followed by a write operation to restore the information or to insert new or modified information.

Ferrites exhibits a second useful nonlinear property that makes coincident-current memories possible. The B-H loop is “square”; i.e., a threshold field exists which must be exceeded before any significant change in flux density can occur. For a given core material and geometry, there is a corresponding thresold current, Isw, which must link the core aperture before the core can be switched. Isw may flow in a single wire or it may be the algebraic sum of currents flowing in several wires through the core. A total of +Isw must flow for a time Tsw to switch the core from – Bs to + Bs (switch from a stored 1 to a stored O). Conversely, the currents must total -Isw for a time Tsw in order to return to the one state, – Br.

A 32k x 17-bit core mat consists of 16 identical bit places. Each bit plane contains 32, 768 cores arranged in a planar array of 128 rows by 256 columns. Each core is threaded by three wires; one of 128 Y-drive lines, one of 256 X-drives, and a sense-inhibit (Z) line that threads all cores in a bit plane. Each X-drive line is series connected to equivalent lines in the other 16-bit planes, as is each Y-drive line. The 17-Z lines are independent. Thus, a 17-bit word location (one core in each bit plane) is uniquely identified by an 8-bit X address, which is decoded to select one of the 256 X-drive lines, and 7-bit Y address to select one of the 128 Y-drive lines.

A word location is interrogated by sending partial read current pulses of amplitude Isw/2 and duration Tsw down the appropriate X- and Y-drive lines. Each of the 17 selected cores at the intersections of the driven lines thus is linked by a total current of +Isw and will be driven to the zero state. A core that was previously in the one state produces an output voltage

on its Z line that is sensed as a one and stored in a data register. A core that was in zero state produces a negligible output so its state is recorded in the data register as a zero. Cores on the driven X and Y lines but not at the intersection are referred to as half-selected, since they are linked by a current + Isw/2, which is insufficient to cause switching. Unselected cores are those not linked by either line.

The subsequent write operation consists of sending current pulses of – Isw/2 (i.e., identical magnitude and duration but opposite in direction to the partial read currents) through the X-Y-drive lines. Each selected core receives a current of – Isw, which is sufficient to switch it to the one state. Those cores that are to store ones (as determined by the bit pattern in the data register) receive only the X- and Y-drive currents. A core that is to store a zero receives a coincident inhibit current pulse of + lsw/2 that is sent through the sense-inhibit wire. The algebraic sum of the three current pulses is thus only – Isw/2, and the core remains in the zero state.

(2) Organization. Figure 1-17 illustrates the organization of a 32k memory module. A 16-bit register stores eight bits to specify the X-address and seven bits for the Y-address (one bit is unused). X- and Y-decoders select the appropriate X-Y-drive lines, which are connected to the read and write (R/W) current generators by the source and sink switches. A 17-bit data register stores the word retrieved from memory during the read operation and enables the appropriate inhibit current generators during the write operation. The MEMIN bus carries the address to the address register and write data to the data register when it is desired to alter the contents of the addressed location. Data read from memory is placed on the MEMOUT bus upon command from the memory controller.

(3) Timing. Operation of the memory is controlled entirely by timing signals generated in the memory controller and fed in parallel to all memory modules. A separate module select line connects each module to the controller. The controller pulls down one of these lines during each memory cycle to select the module to be accessed. Figure 1-18 shows the time relationships of these signals, which are all negative true. Read-modify-write exemplifies memory operation. Read-restore and clear-write are special cases of this basic cycle.

A read-modify-write cycle begins with the controller placing a 15-bit address on bits 0-15 of the MEMIN bus and issuing a strobe, MAST, which loads all memory address registers. Bits 1-7 select a Y line and bits 8-15 select an X-line. Subsequent timing signals are gated by the MOSL signal so that only the selected module is activated.

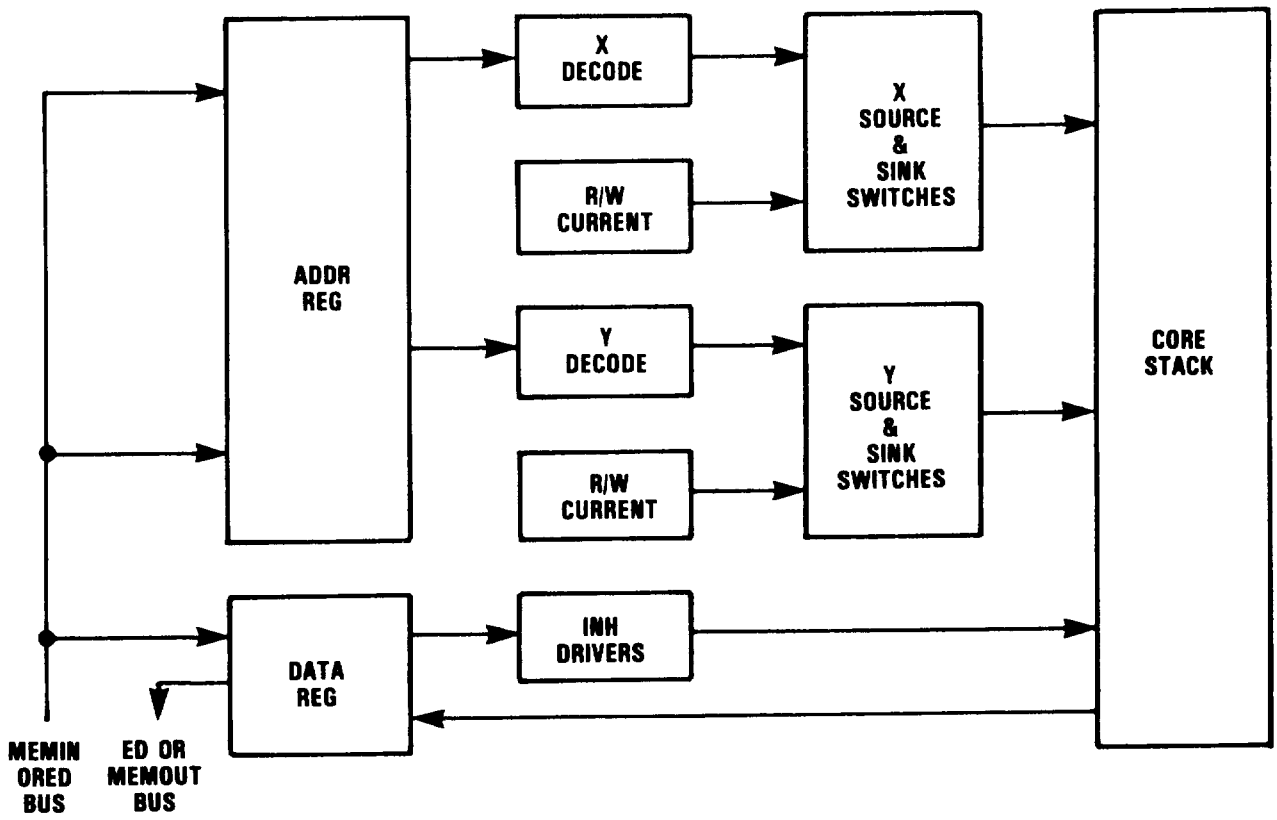

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Figure 1-17. 32k Core Memory Module, Simplified Block Diagram

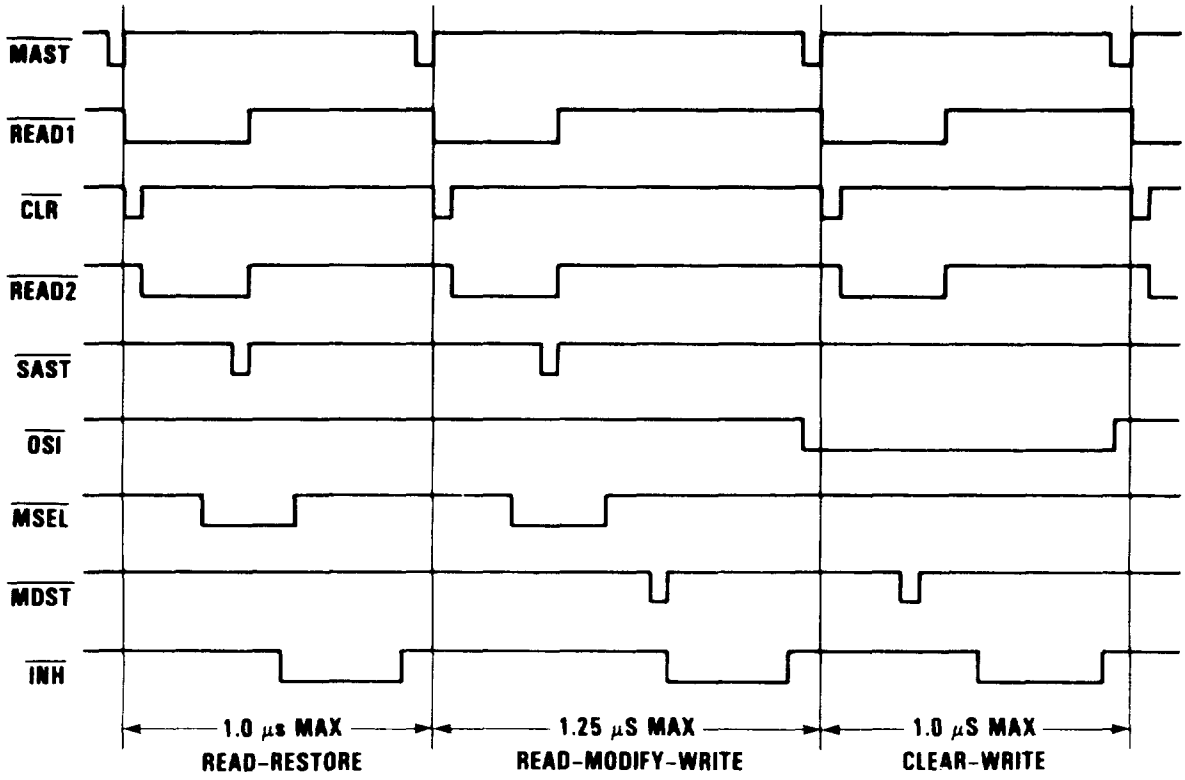

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Figure 1-18. Memory Timing Signals

READ1 and READ2 turn on the Y-and Z-read-current generators, respectively, READ1 begins 50 nS before READ2 to minimize the effect of noise perturbations from half-selected cores on the desired outputs. All bits in the data register are cleared by the CLR signal at the start of READ1. Sense amplifiers, connected to the 17 sense-inhibit lines, translate the low-level core outputs to the TTL-compatible signals. SAST, which is generated in the memory to coincide with the peak core outputs, gates the sense-amp outputs to the preset inputs of the data register, Cores switched from the one state set their corresponding bits in the data register to ones; those that were already in the zero state produce outputs below the sense-amp threshold, and consequently do not alter the states of the associated data register bits. MSEL places the contents of the data register on the MEMOUT or ED bus at the end of the read operation.

Following the read half cycle and after the CPU has performed whatever operations are required on the word retrieved, the modified data is placed on the MEMIN Bus or ED bus and loaded into the data register by MDST. INH turns on the write-current generators and activates those inhibit drivers whose controlling bits in the data register are zeros.

The read-restore cycle differs only in the absence of MDST since the data retrieved is written back into core. In a clear-write cycle, SAST and MSEL are absent since the previous contents of the address selected are not used.

(4) X-Drive. The X-drive includes the SAST generator, a dual current source to generate the Z-read and write currents, a dynamic bias (DB) generator, an 8-bit address register, 16 dual source-sink switches to route the drive currents to the X-line specified in the address, and four 3-to-8-line decoders to select the proper source and sink switches.

(5) Y-Drive. The Y-drive is substantially the same as the X-drive except that it contains data registers and inhibit current generators for the nine even numbered bits. In addition, the proper A-B decode signal (81 or 62), is also fed to the X-drive board. In contrast to the X-drive, the Y-drive uses only four dual source-sink switches and only three 3-to-8-line decoders. This is due to the fact that the Y-dimension contains only 128 lines as compared to 256 for the X-drive. Bits 1-4 of the address select one of 16 paths to the stack, and bits 5-7 select one of eight return paths.

1-19. SEMICONDUCTOR MEMORY DESCRIPTION

Semiconductor memory is contained wholly within the processor chassis. The minimum configuration consists of an ERCC PCB, a memory controller PCB, and a 64 kW storage array PCB. An additional 64 kW array can be added to this configuration. The addition of one or two 64 kW arrays in excess of 128 kW requires the addition of a second memory controller. The maximum configuration is 256k words of storage, two memory controllers and one ERCC PCB.

a. Memory Organization. The following paragraphs describe how memory is partitioned in terms of the addressing structure, as an introduction to the various functions of the memory controller.

Each 64k word board is partitioned into two groups (0 and 1), each containing 32k words. Each board is also divided into two modules, either A or B, or C or D, as shown in figure 1-19. If a single 64 kW array is installed, it has modules A and B, if a second is installed, it has modules C and D, with respect to a memory controller. A fully complemented memory has two sets of A, B, C and D modules. Each module within a group contains 16k words (Module A0, A1, 60, 61, C0, C1 D0, D1).

The storage elements (RAMs) are 16k x 1-bit devices. Each module within a group consists of 21 RAM devices, to provide a 21-bit word (16 data bits + 5 error code bits). To address 16k memory locations requires 14 address bits; however the RAMs only have seven address lines. The geometry is so arranged to provide 128 columns each consisting of 128 rows. To select a particular location (memory address) the row address is sent first, followed by the column address (figure 1-19). Each memory controller PCB is jumpered to recognize its own address and also to determine whether 2-way or 4-way address interleaving is required. This addressing scheme is shown in figure 1-20. If one 64k word board is installed, 2-way interleaving is imposed. If two 64k word boards are installed, 4-way interleaving is imposed. In 192k word systems, controller 1 is jumpered for 4-way interleaving and controller 2 is jumpered for 2-way interleaving. In 256k word systems, both controllers are jumpered for 4-way interleaving.

b. SC Memory Controller, Model 1753. The controller performs the following functions

- Address decoding, including module address timing and generation, row and column address generation and timing (sequencing).
- Interface timing generation and interleave control.
- Write data buffering.
- Refresh address generation and refresh timing.

Clock generation is performed on the ERCC board and required clocks are buffered on the controller board.

c. 64 kW Semiconductor Array. If a single 64 kW array is installed with a memory controller, the array will contain modules A and B, which are identified as A0, A1, B0, B1. If a second 64 kW array is installed, it will contain modules C and D, which are identified as C0, C1, D0, D1. A 16 kW segment is either A0 or C0, A1 or C1, B0 or D0, B1 or D1. Each 64 kW array consists of control buffers, address buffers, a data-in bus, four 16 kW arrays, a data-output multiplexer, and a data-out bus.

1-20. POWER SUPPLY (AC AND DC) DESCRIPTIONS

a. Power Connection. A single connector (J1) on the front panel of the processor chassis accommodates either ac or dc power input. If an ac input is used, the dc pins are not connected, and vice versa. For further details on power connection refer to Chapter 3. The optional battery back-up supply, if used, sustains semiconductor memory in the event of input power disruption. The optional battery supply is connected to J6 on the processor chassis front panel.

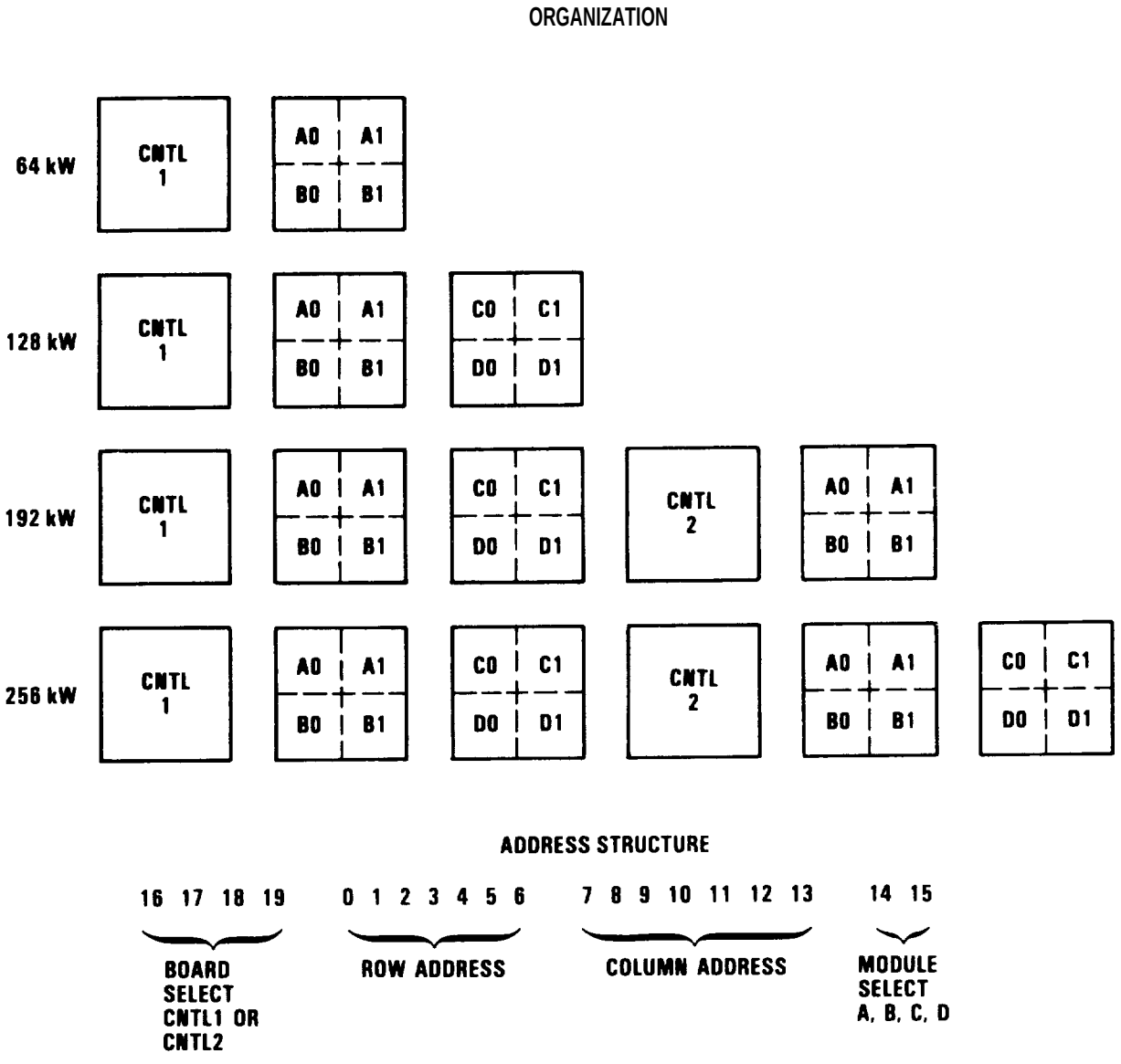

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Figure 1-19. Memory Organization

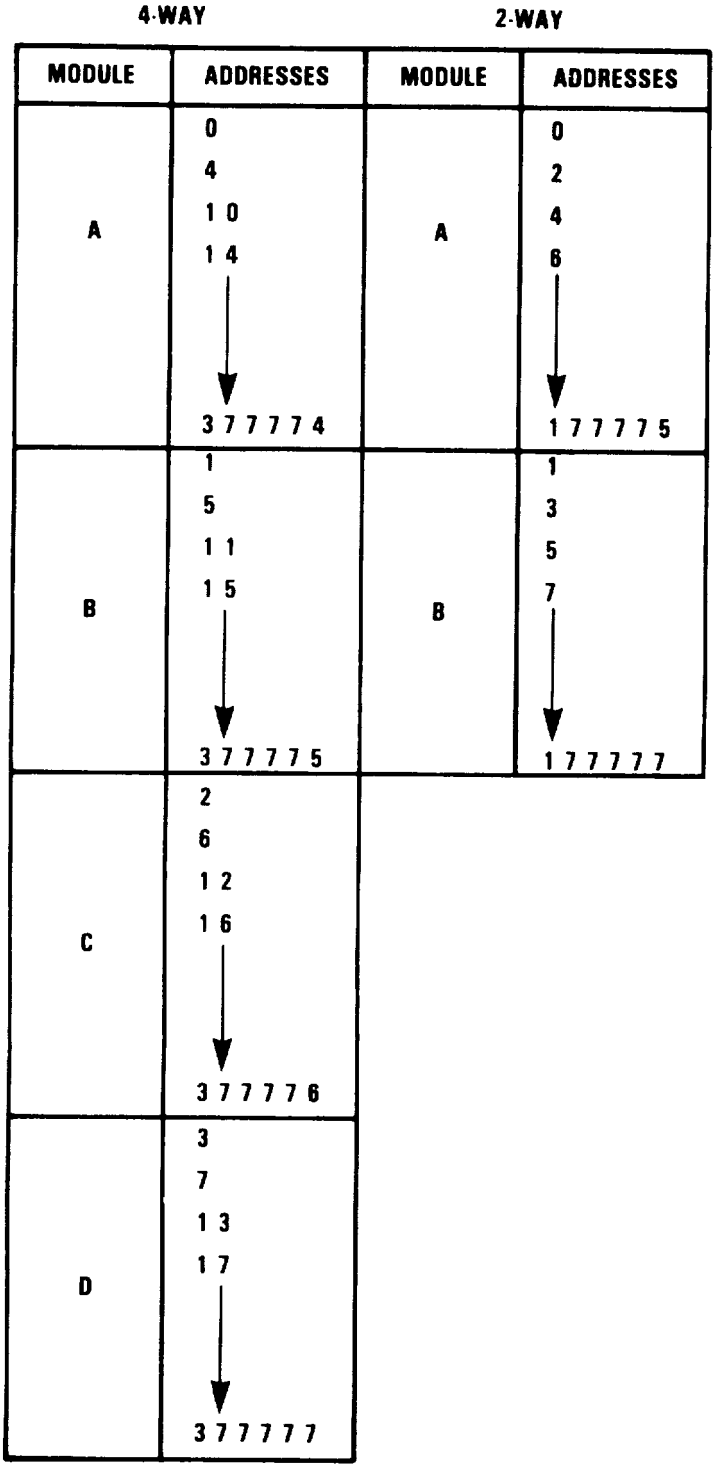

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Figure 1-20. Address Interleaving

b. Fusing. Power is separately fused for ac and dc input. Three-phase ac input is protected by fuses F1, F2, and F3 (10A). Single-phase ac input is protected by fuses F1 and F2 (10A), and dc input is protected by fuses F4 and F5 (30A or 35A).

NOTE

A blown F4 or F5 fuse indicates reversed polarity either at the power input to the processor chassis or at the source.

c. EMI Filtering. A EMI line filter is connected between the fuses and the power supply to reduce conducted interference on the input supply lines. The dc EMI filter is Model 3884. Model 3883 EM I filter supports 115/220 V ac, single-phase input power configurations. Model 3883A accommodates 115/220 single-phase and 115/220 or 208 V ac, three-phase operations. A chassis configured for ac operation contains an ac power supply, ac fan, and ac filter. To reconfigure a chassis for dc operation, the power supply, the ac fan, and the filter must be changed. Also, a change in the ac input may require a jumper change and a change in the fan type. Additional filtering, internal to the power supply, reduces the level of conducted interference generated by the power switching circuits.

d. Model 5617 AC Power Supply. The model 5617 power supply operates from single-phase or three-phase power. A block diagram of the model 5617 ac power supply is provided in figure 1-21.

e. Model 5687 DC Power Supply. The model 5687 power supply operates from a nominal 28 V dc. Supply regulation occurs over the steady-state of 22 V to 36 V, and tolerates short-term transients to 54 V. Input power requirements range from 350 W to 575 W, depending on processor chassis configuration. A block diagram of the Model 5687 dc power supply is provided in figure 1-22.

1-21. INTERNAL ELECTRICAL CONNECTIONS

a. Front Panel Connectors. In the Processor systems applications, connector J6 (figure 1-5) is used to interconnect the processor with a remote memory chassis (RMC) and/or a battery backup power supply.

b. EMI Filters. The EMI filter input connector (J30) mates with front panel connector P-30 and the filter output connector (J31) mates with the chassis motherboard connector P31. These connectors are shown in figure 1-23.

c. Power Supply Internal Connections. Power is provided to the chassis through front panel connector J1, which is connected through the fuses and EMI filter to connector J 14 on the back bulkhead of the chassis (fig. 1-24): Connector J 14 mates with connector P14 on the power supply to provide primary input power (fig. 1-24 or 1-26). Regulated voltages are routed to the motherboard through power supply output connector P15.

Connector P15 mates with chassis connector J15. An interconnection diagram is given in figure 1-27. Power for an external blower is provided through chassis connector J17 (fig. 1-24).

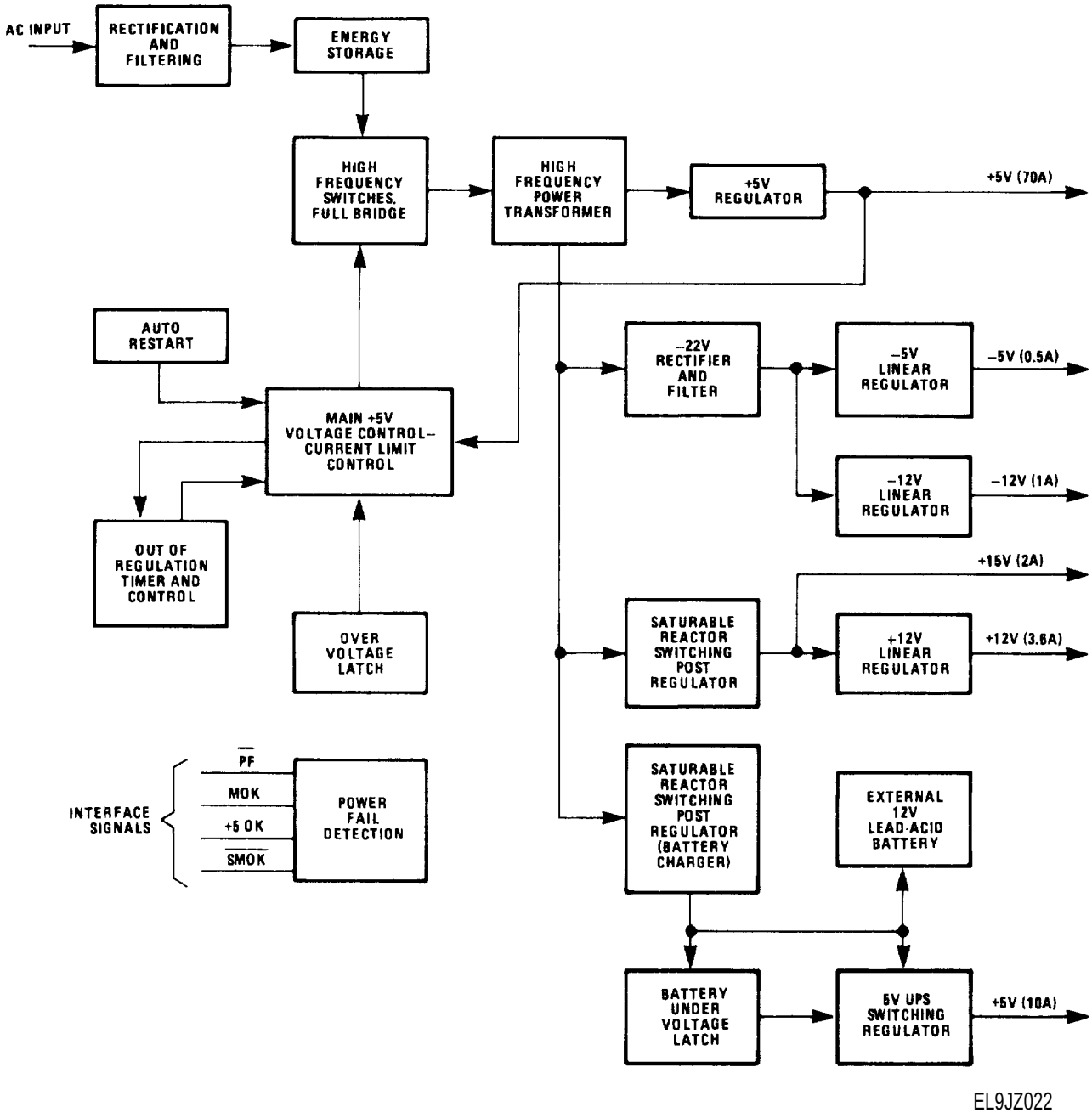
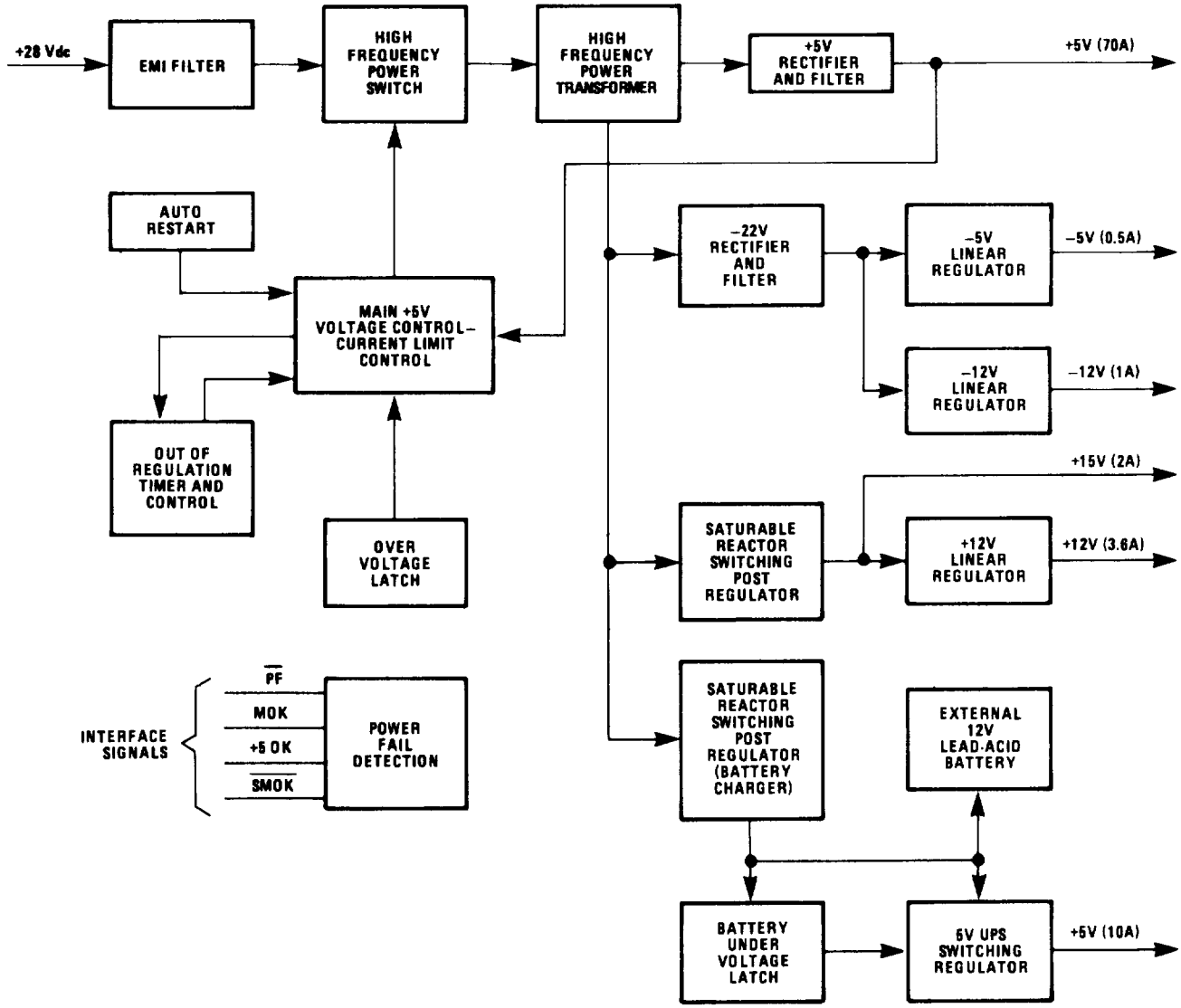


Figure 1-21. Model 5617 AC Power Supply, Simplified Block Diagram



EL9JZ023

Figure 1-22. Model 5687 DC Power Supply, Simplified Block Diagram

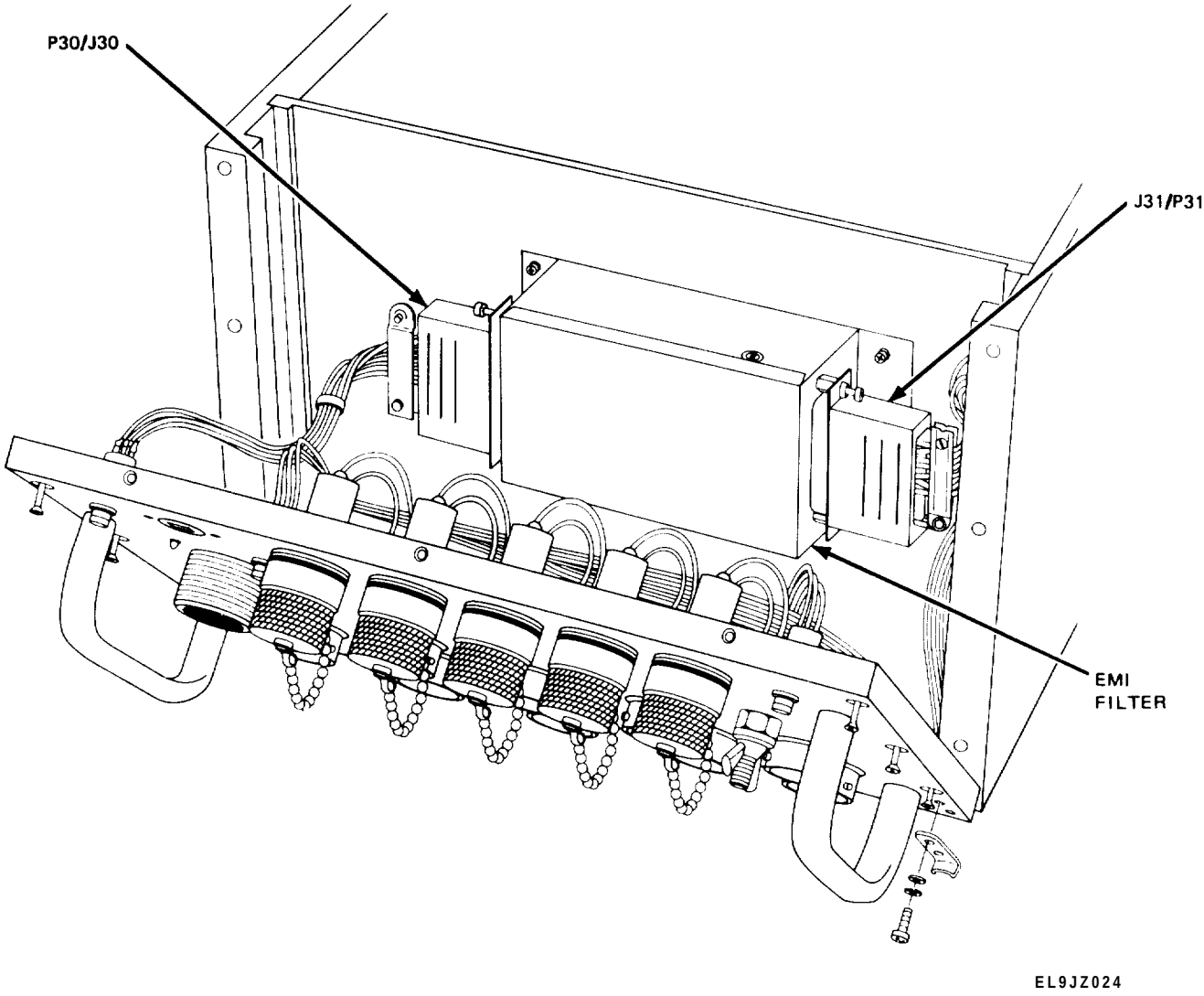


Figure 1-23. EMI Filter and Connectors

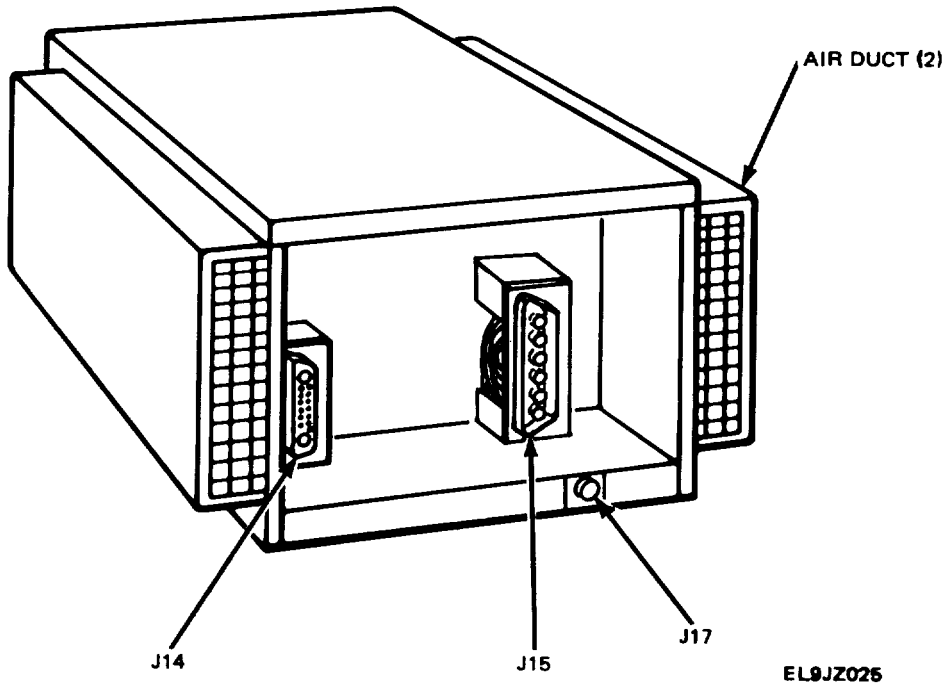


Figure 1-24. Chassis Connectors for the Power Supply

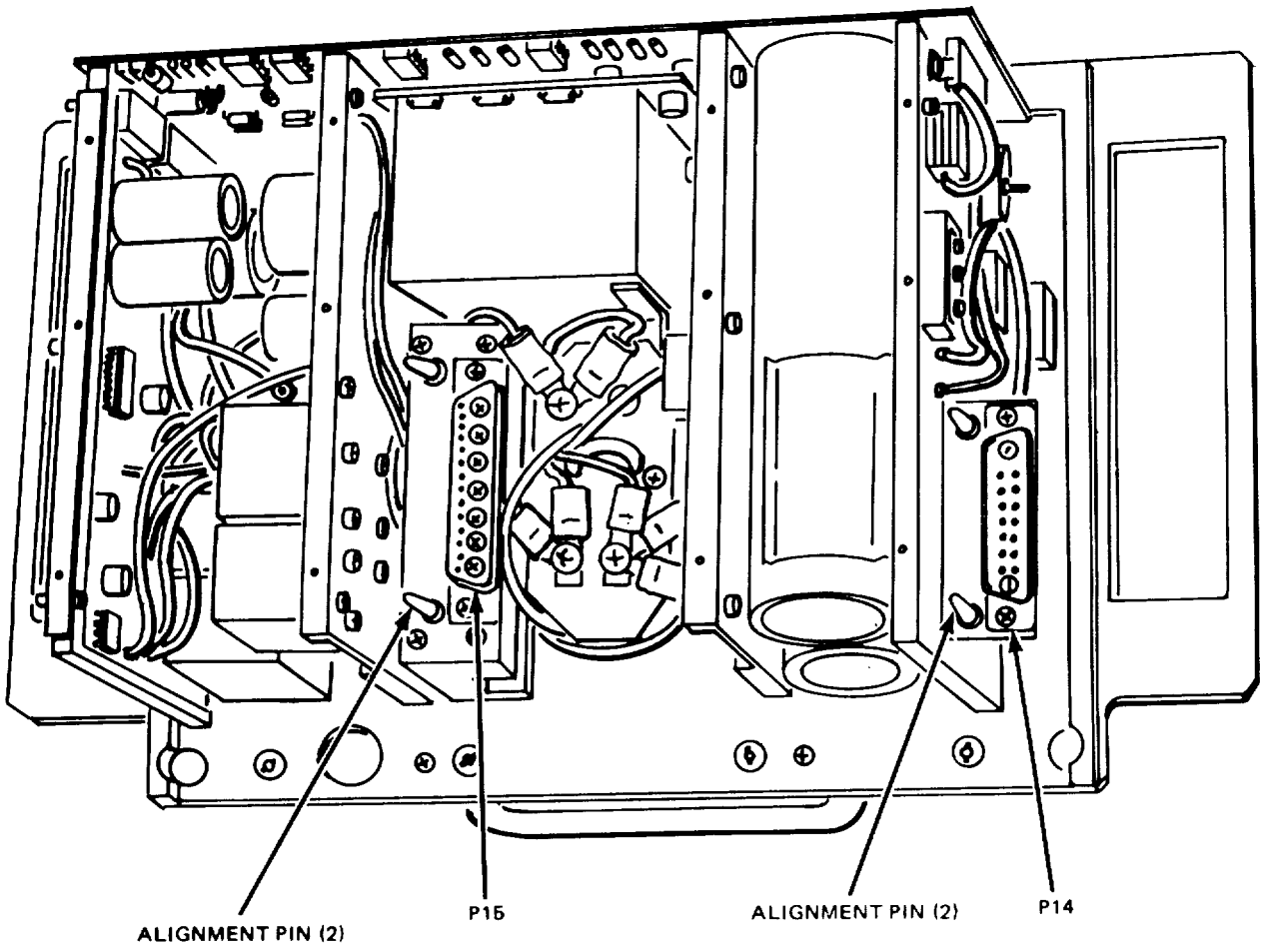
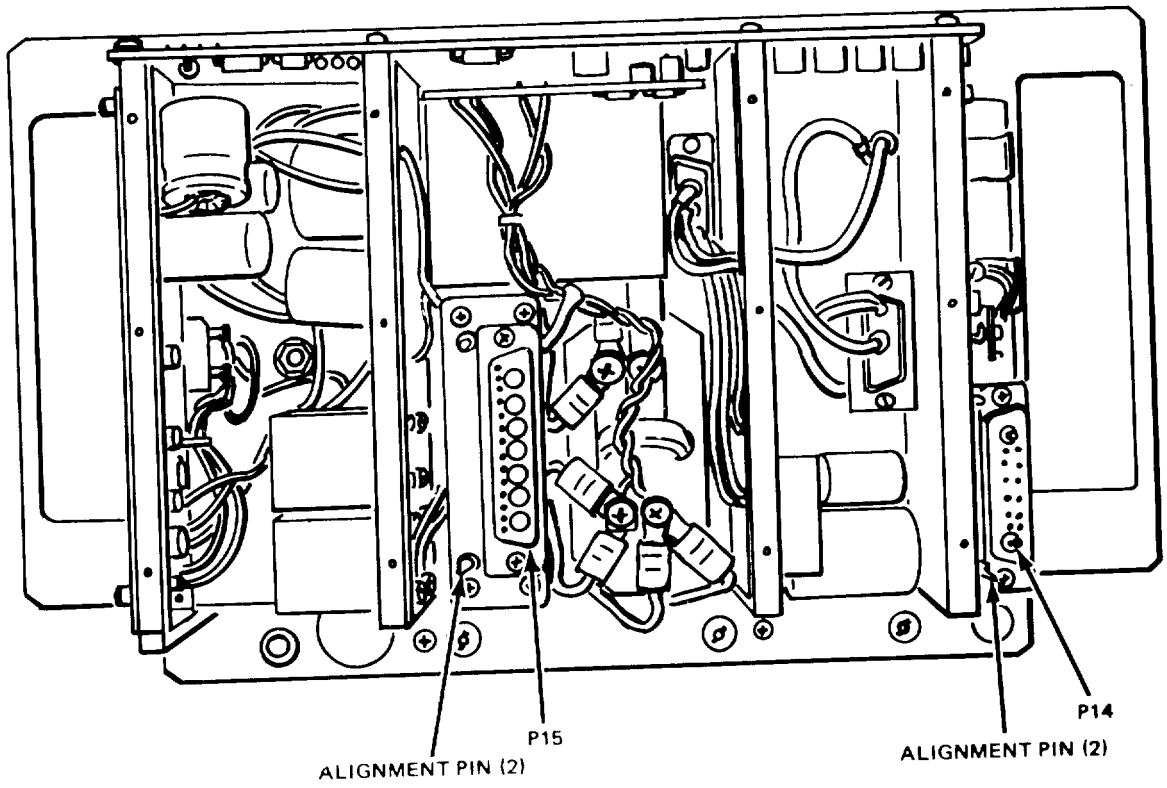


Figure 1-25. Model 5617 AC Power Supply, Component View (Motherboard Removed)



EL9JZ027

Figure 1-26. Model 5687 DC Power Supply, Component View (Motherboard Removed)

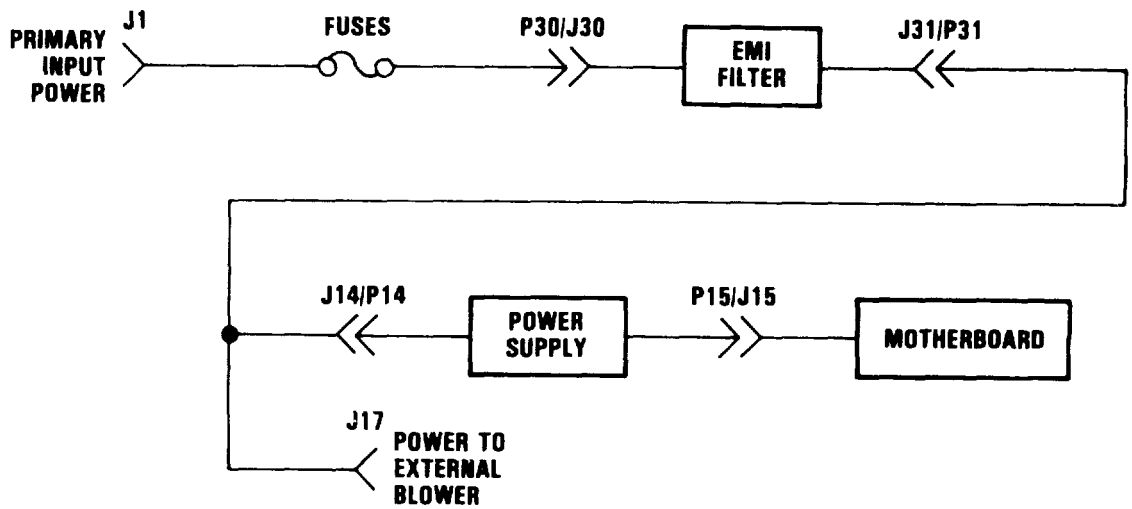


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Figure 1-27. Power Supply Interconnection Diagram

Motherboard Wiring. A motherboard (MB) is a multilayer printed circuit board (PCB) which contains the interconnections between plug-in circuit modules. Each PCB has two connectors, PI and P2, for making corresponding electrical connections to J1 and J2 connectors on the motherboard, as shown in figures 1-28 and 1-29. In figure 1-29 note that the connector pins are arranged in three rows, A, B, and C, and are numbered 1 through 32 (i.e., the first pin is A-1 and the 96th pin is C-32). Motherboard connectors are thus designated by location as A1J1, A1J2, A2J1, etc., and the reference designations are in sequential order throughout the assembly.

A complete motherboard assembly actually consists of two motherboards installed on the same plane. The larger motherboard assembly is the CPU-I/O motherboard which is the same in both core memory and semiconductor memory installations. The smaller motherboard is the memory motherboard, which is dedicated to the type of memory installed. In addition, interconnections between the two motherboards vary according to the type of memory installed. Appendix G provides core memory and semiconductor memory motherboard connection lists.

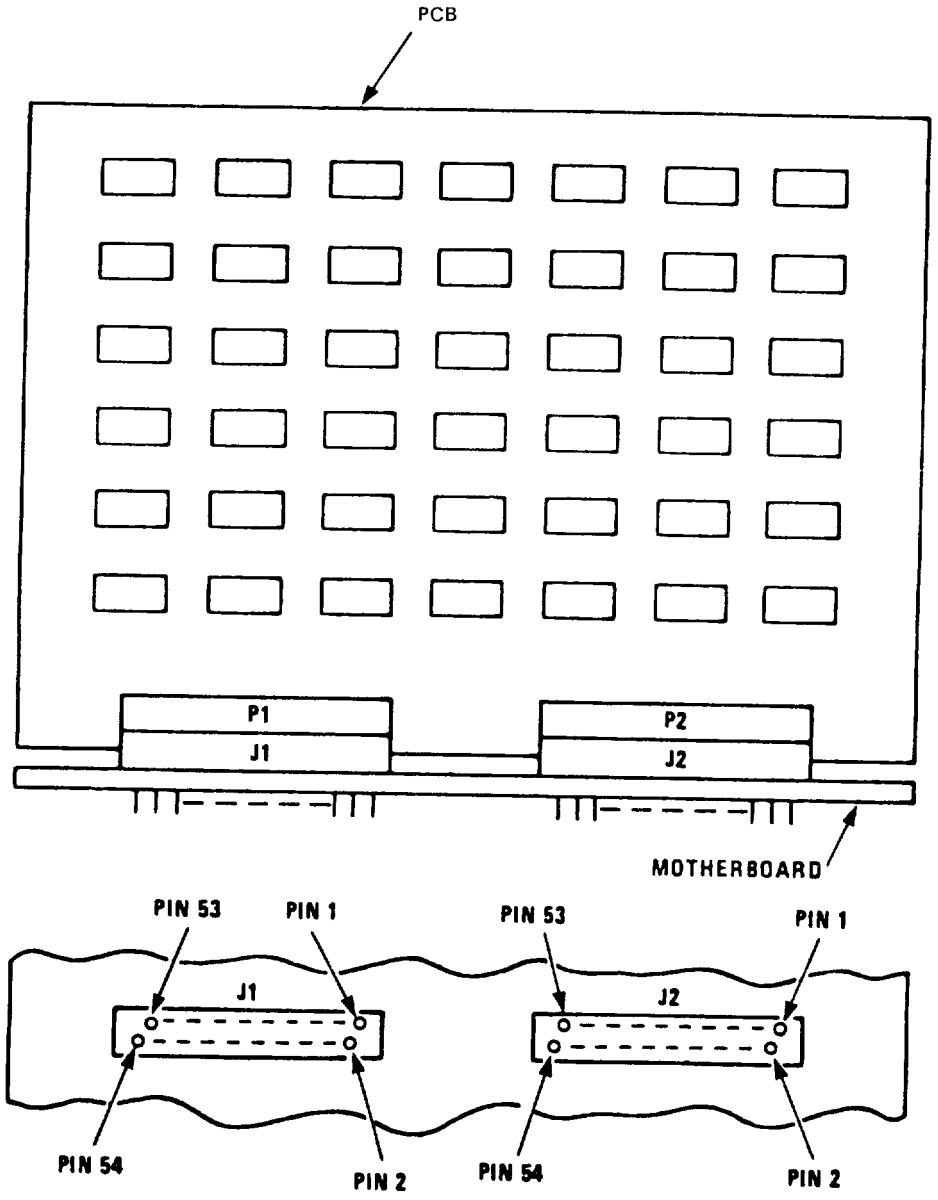
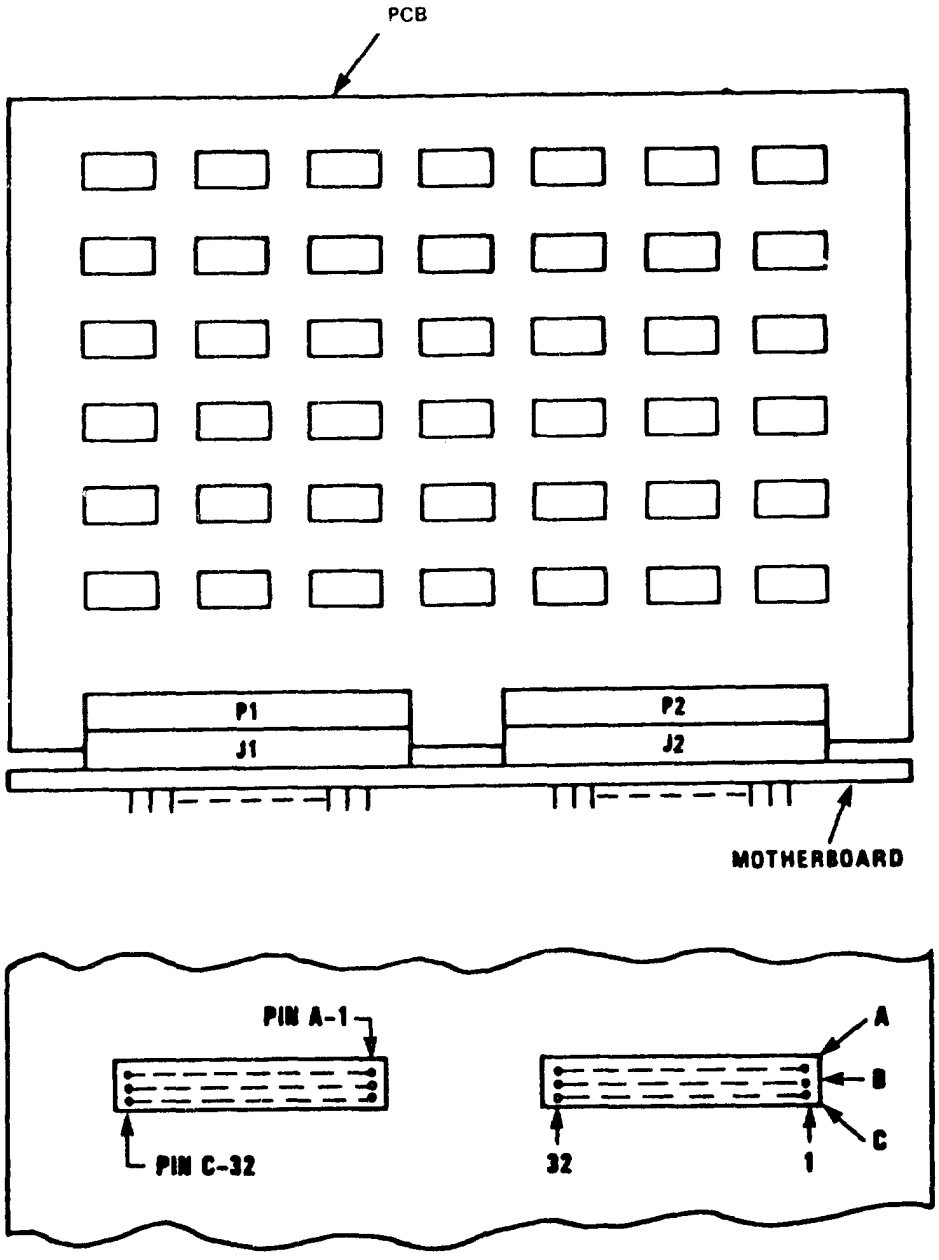


Figure 1-28. Motherboard Connector Pin Layout, 54-Pin



EL9JZ030

Figure 1-29. Motherboard connector Pin Layout, 96-Pin

CHAPTER 2

RECEIVING INSPECTION

2-1. GENERAL

This chapter provides instruction for visual inspection of the processor received from organizational maintenance before starting any corrective actions. Records and forms are checked upon receipt of the unit. Then the unit is subjected to a visual inspection and a determination is made of the appropriate corrective action.

2-2. EQUIPMENT TAGS AND FORMS

NOTE

Printed circuit boards (PCBs) from different processors have different jumper configurations as listed in Table 1-4 and appendices C, D and E. This information is important when troubleshooting or analyzing failure cause.

Equipment tags and forms are checked when the processor is first received, and before any inspection or other action is accomplished. Ensure that the forms are completely filled out. Verify that the unit identified on the forms is the unit that was actually received. If the unit is a PCB, ensure that the original host processor configuration is identified (i.e., (V) 1, 1X, 2, 2X, 3, 3X, 4, or 4X).

2-3. UNPACKING INSTRUCTIONS

The processor, its power supply and its PCBs, will normally be received packed separately. Unpack the shipping/storage containers as follows:

WARNING

The processor is a heavy piece of equipment. Always use three technicians when moving or lifting the unit to prevent injury to personnel.

a. Unpacking.

(1) Open shipping cartons and remove equipment.

(2) Place equipment on a suitable clean and dry surface for inspection.

(3) Keep all shipping materials for use in repacking and shipping/storage.

b. Checking Unpacked Equipment.

(1) Inspect the equipment for possible damage that may have been incurred during shipment. If the equipment has been damaged, report the damage on SF 364, Report of Discrepancy (ROD).

(2) Check the equipment against the packing slip to ensure the shipment is complete. Report all discrepancies in accordance with the instructions of TM 38-750.

(3) Check to see whether the equipment has been modified; review accompanying documents.

2-4. VISUAL INSPECTION

A visual inspection is performed on the received processor to determine what corrective action is required. The following paragraphs describe visual inspection points on a chassis, power supply, or PCB. Perform all or any of the procedures as applicable.

a. Chassis Inspection. Perform the following checks whenever a processor is received for repair. Write down any detected damage or questionable conditions.

Chassis exterior	Physical damage or distortion Corrosion, dirt, or other material
Finish	Nicks, dents Abrasions or scratches
Hardware	Handles loose, damaged, or missing Screws missing or damaged Unauthorized attachments or modifications
Panel markings	Illegible or incorrect markings Unauthorized markings Missing markings
Identification plate	Insecure attachment Illegible information Missing or damaged plate
Front panel	Panel markings clear and readable Unauthorized markings Connector security Damage to connector pins, insulation, or hardware

Chassis interior (Includes HDA Tray)	Dust, dirt, or foreign material Corrosion Motherboard condition Wiring condition PCB connector condition Power supply connectors condition (power supply removed)

b. Power Supply Inspection. Inspection items for both ac and dc power supplies are identical. Write down any detected damage or questionable conditions.

Rear panel	Bent or broken cooling fins Missing or damaged captive mounting screws Condition of anodized finish
Electronics	Security of subassemblies on chassis Burnt, loose, or discolored components Burnt, broken, or discolored wires

c. Printed Circuit Boards (PCBs). Inspection is intended to detect obvious major damage or defects. Write down any detected damage or questionable conditions.

PCB	PCB integrity for cracks or damage Heat sink security around edge
Connectors	Securely attached to PCB Bent, broken, or missing pins
Components	Evidence of overheating or other damage Jumpers installed properly and soldered securely

2-5. ITEM DISPOSITION

Disposition of the processor following visual inspection depends upon the amount and type of damage, if any, discovered. If no damage is discovered, the item is scheduled for testing. If obvious damage is present and repair is within the capability of direct support/general support or special repair activity (SRA) capabilities, the item is scheduled for repair of the obvious defect before testing. If major damage is discovered, damage that is beyond direct support/general support or SRA capability, the item is packed as described in chapter 5 and sent to depot for repair or disposition as applicable.

a. Chassis Repair Guidelines. Chassis repairs at direct support/general support maintenance are limited to minor wiring repairs, connector repairs, and minor touchup of the finish and front panel markings. Any repair beyond this scope requires the chassis to be shipped to depot.

b. Power Supply Repair Guidelines. Direct support/general support repair of power supplies is limited to tightening any loose hardware and minor touchup of the finish. All electronic testing and repair activity is performed at Depot.

c. PCB Repair Guidelines. All PCB repair, except for core memory modules, is performed at the SRA facility. Core memory modules are depot repair items and are routed to depot, regardless of their condition.

CHAPTER 3

DIRECT SUPPORT MAINTENANCE INSTRUCTIONS

Section I. GENERAL INFORMATION

3-1. GENERAL

This chapter discusses the direct support maintenance concepts and provides instructions for maintaining the Data Processing Set AN/UYK-64(V). Included in this chapter are troubleshooting instructions, troubleshooting flowcharts, and testing procedures (including maintenance diagnostic program information).

The processor is a sophisticated and complex piece of electronic equipment. Isolation of failures to the circuit component level usually requires the services of a thoroughly trained technician; however, the modular construction of the processor allows straightforward isolation of failures and easy replacement at the module level.

There are three basic approaches to maintenance planning; the optimum approach depends on the specific requirements of each application.

a. Chassis Replacement. In the event of a failure, an entire unit is replaced with a spare operational processor. This method minimizes mean-time-to-repair (MTTR), which can **be a matter of** seconds. The failed unit is then forwarded to the appropriate level of maintenance for repair. This approach is especially attractive for installations with several identical processors or installations having spare units.

b. Module Replacement. In the event of failure, the fault is localized and isolated to a replaceable module (assembly, subassembly, or major component), and a spare module is installed. MTTR with this method is usually less than an hour. This approach is economically preferable to unit replacement (para a above) in those installations with several processors of differing configurations. The failed module is forwarded to the appropriate level of maintenance for repair or replacement,

c. Component Replacement. In the event of failure, the fault is localized and isolated to the failed component, which is then replaced. This approach is not attempted except at general support maintenance, special repair activity (SRA) facilities, or at depot maintenance. Refer to the Maintenance Allocation Chart (MAC) in TM 11-7021-202-12. Component replacement requires considerable technical skill, sparing of a large number of component types, and can require hours of troubleshooting and repair time.

3-2. INSPECTIONS

The processor requires a minimum of periodic inspection and maintenance. Refer to the MAC and the preventive maintenance checks and service (PMCS) contained to TM 11-7021-202-12.

If the processor operates in a vibration environment (e.g., a moving vehicle), an occasional check of external screw tightness is performed. In particular, the screws holding the side rails on the PCBs conductive heat path are tightened. A visual inspection of the system cables and connectors is also made prior to each deployment.

When the processor has not been operated for some time, it is checked out in an operational system configuration before use. Refer to paragraph 3-12.

Section II. REPAIR PARTS, SPECIAL TOOLS, TMDE, AND SUPPORT EQUIPMENT

3-3. TOOLS AND TEST EQUIPMENT

Tools and test equipment required for direct support maintenance of the equipment are listed in the Maintenance Allocation Chart (MAC) in TM 11-7021-202-12.

3-4. SPECIAL TOOLS, TMDE, AND SUPPORT EQUIPMENT

Special tools, TMDE, and support equipment are listed and illustrated in the repair parts and special tools list (RPSTL) TM 11-7021-202-34P covering direct support maintenance for this equipment.

3-5. REPAIR PARTS

Repair parts are listed and illustrated in the repair parts and special tools list (RPSTL) TM 11-7021-202-34P, covering direct support maintenance for this equipment.

Section III. TROUBLESHOOTING

3-6. INTRODUCTION

This section provides troubleshooting information for locating, isolating, and correcting equipment malfunctions. Included are troubleshooting flowcharts and procedures, and instructions for loading and running diagnostic tests.

NOTE

This manual cannot list all malfunctions that might occur, or all tests, inspections, and corrective actions required. If a malfunction is not listed, or is not resolved by the listed corrective actions, notify the shift supervisor.

NOTE

The procedures and instructions in this section are a continuation of the troubleshooting information found in chapter 4 of the operator's and organizational maintenance manual TM 11-7021-202-12 for the processor.

Procedures contained in this section are used for determining which replaceable module has failed in an inoperative processor. Replaceable modules in the processor are the power unit assembly, ac power unit (electronics module), power supply, printed circuit boards (PCBs), EMI filter, some wiring and cabling, and fuses. Also certain chassis/mainframe components are replaceable at direct support and/or general support maintenance. In core-based processors, each 32k memory increment consists of three PCBs: Y-driver, X-driver, and a 32 kB word stack. The individual PCBs are not interchangeable with other PCBs of the same type and are not replaced individually; each 32K memory increment is factory matched and balanced and must be replaced and serviced as a module (unit).

Whenever an apparent processor malfunction occurs, it is usually wise to spend a few minutes eliminating the possibility of operator error (e.g., program not properly loaded, peripheral equipment not connected, etc.) or programming bugs in unproven software. If processor failures seem probable, there are two basic tools in fault isolation: operating the processor in the system mode through the system terminal, and running the diagnostic programs. Operating the processor in the system mode and exercising the various commands allows the maintenance technician to check a significant portion of computer hardware. This generally will lead the maintenance technician to isolate a failure to the CPU, memory, or power supply. If operating the processor in the system mode does not isolate the failure, then the diagnostic programs are run. The diagnostic programs are useful in two ways: first, they often simplify identification of the failed module; second, they are a thorough verification of correct hardware operation. It should be noted that since there are only a few replaceable units in the processor, the trial-and-error substitution is viable.

When using this approach, first test all power supply voltages and level detectors in semiconductor memory installations with battery back-up to make sure the batteries are fully charged. If the voltages are incorrect, replace the power supply. If the voltages are correct, then the fault is probably not in the power supply.

a. Power Supply Shutdown. Because overcurrent, overvoltage, and overtemperature sensors protect the power supply from externally caused failures, actual supply failure should be rare. However, many problems are at first diagnosed as power supply failures, since the supply reaction to an overstressed condition, whether it be temperature, voltage, or current, is to set a latch which electronically shuts down all outputs. The following subparagraphs outline techniques for separating actual supply failures from apparent supply failures. Should an actual supply failure be diagnosed, the supply is returned to the depot maintenance for repair.

The EM I filter and the power input tuses (fig. 3-1) are checked before troubleshooting the power supply. A blown fuse indicates a probable fault in the EMI filter or in the power supply. If power is present at the output of the EMI filter, proceed with troubleshooting the power supply. Refer to chapter 1 for power supply operating principles.

NOTE

Separate connector pins are used for ac and dc power, and power system continuity is maintained only when the power supply and the EMI filter are both ac or dc, as required. Refer to tables 3-1 through 3-4. See figures 3-1 and 3-2.

(1) Overcurrent Shutdown. A current-sensing resistor in series with the emitters of the chopper transistors is used to monitor the total load current. A short on either the +-5 V or + 12 V output (e. g., due to a shorted tantalum capacitor) will cause this current to exceed a preset threshold and cause the chopper to shut down. A short on either the -5 V or -12 V output probably will not cause the threshold to be exceeded; however, both of these outputs are current-limited so that a short on either will effect only that output and not the others.

To isolate a circuit module that is overloading one of the outputs, remove the modules one at a time. If the short is on -5 V **or -12** V line, the voltage will return **to** the proper value when the faulty module is removed. If the short is on the + 5 V **or + 12** V line, the latch must be reset by turning the power off and back on each time a module is pulled. When the faulty module is pulled, the supply will come on and stay on.

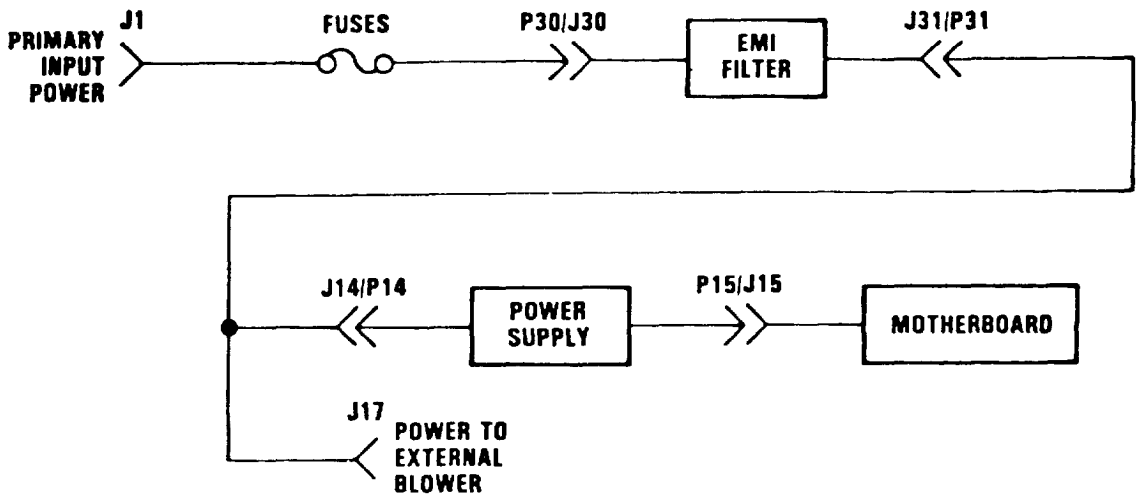
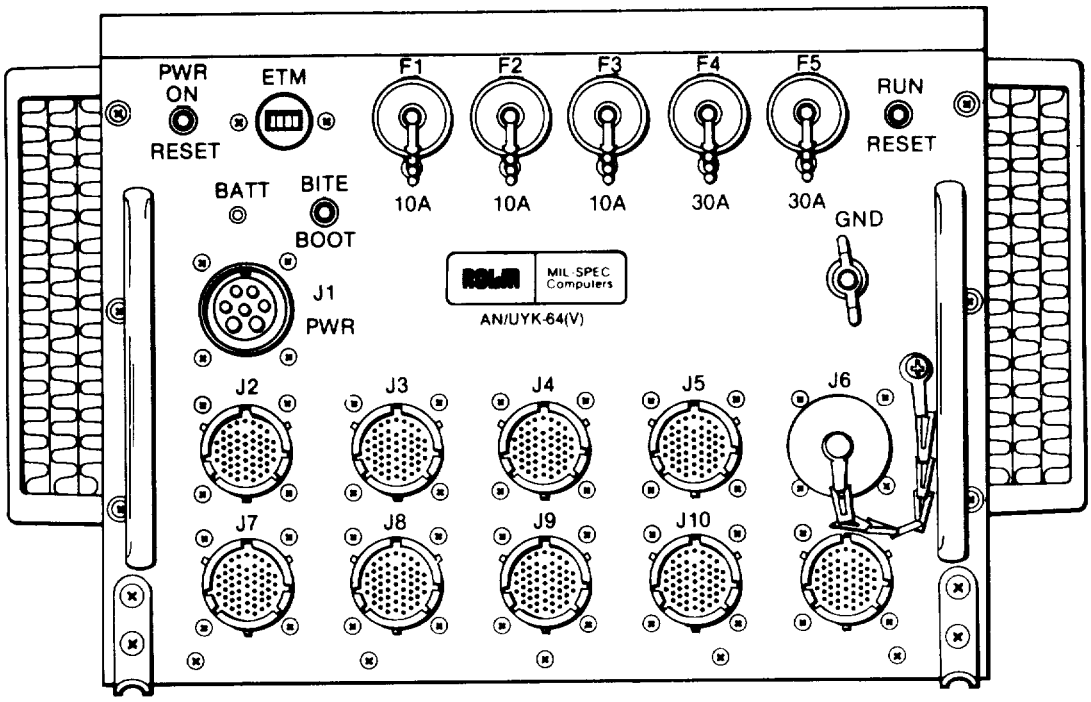
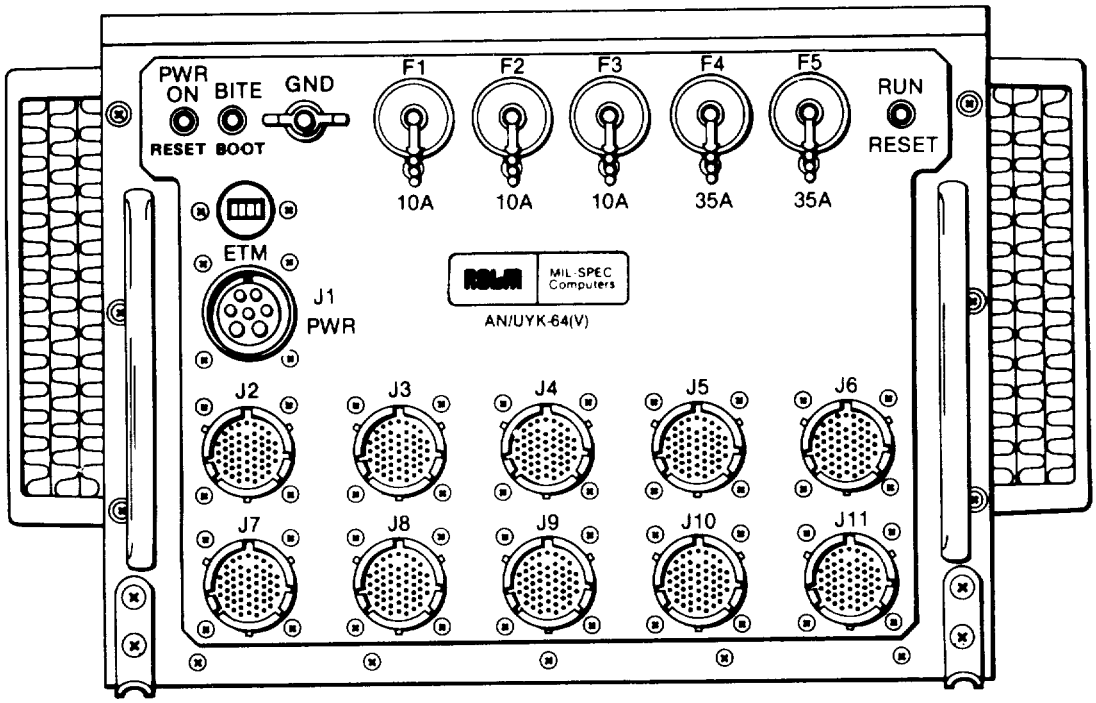


Figure 3-1. Power Supply interconnection Diagram



SEMICONDUCTOR- BASED PROCESSOR (V1, V1X, V3, V3X)



CORE-BASED PROCESSOR (V2, V2X, V4, V4X)

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Figure 3-2. Front Panels for Core and Semiconductor Processors

Table 3-1. Power Connector J1

Pin	Function
A	- 28V
B	AC Phase B
c	AC Phase C
D	+ 28V
E	AC Phase A
G	Chassis Ground

Table 3-2. Battery Backup Connector J6

Pin	Function
A	+ BATT IN
B	+ BATT IN
C	BATT RET
F	BATT RET

Table 3-3. EMI FIlter Internal Connections, Input

Input (J30) Pin No.	Function		
	Model 3383 (ac)/1-Phase	Model3883A(ac)/3-Phase	Model 3884(dc)
A1	NC	NC	+ D C
3	AC Phase A	AC Phase A	NC
4	AC Phase B	AC Phase B	NC
5	NC	AC Phase C	NC
6	Chassis Ground	Chassis Ground	NC
10	AC Phase A	AC Phase A	NC
11	AC Phase B	AC Phase B	NC
12	NC	AC Phase C	NC
13	Chassis Ground	Chassis Ground	NC
A2	NC	NC	- DC

Table 3-4. EMI Filter Internal Connections, Output

Input (J30) Pin No.	Function		
	Model 3383(ac)/ 1-Phase	Model 3883A(ac)/ 3-Phase	Model 3884 (dc)
A1	NC	NC	+ DC
3	AC Phase A	AC Phase A	NC
4	AC Phase B	AC Phase B	NC
5	NC	AC Phase C	NC
6	NC	NC	NC
10	AC Phase A	AC Phase A	NC
11	AC Phase B	AC Phase B	NC
12	NC	AC Phase C	NC
13	NC	NC	NC
A2	NC	NC	- DC

(2) Overvoltage Shutdown. The shutdown latch will also be set if a transient on the input approaches a level that could damage the supply, or if either the + 5 V or +12 V output should rise to a level that could damage circuit modules. The latter condition could be caused by a regulator loop failure or instability, which would necessitate repair of the power supply. It could also be caused by a wiring or connector problem that would open one of the remote sense connections. If the latch is tripping and no shorts can be found, the sense line for the + 5V or + 12V output is checked for continuity.

(3) Overtemperature Shutdown. A thermistor inside the supply is used to monitor the internal supply temperature and shut down at about 100°C. If a maintenance technician is present when shutdown occurs, the problem is obvious. The technician need only touch the chassis to identify the problem. Should the shutdown occur on an unattended machine, it may cool down before the problem is noted. Upon restarting a machine that has had an unexplained shutdown, the technician always ensures that the fan is operating and that the air intake port is not blocked and air flow around the unit is not inhibited in any way.

(4) Obvious Supply Failures. Since the electronic shutdown circuits protect the processor electronics and most of the power supply components, a blown fuse generally means that there has been a hard failure in the input circuitry or in the control section of the supply. It is possible, particularly in heavily loaded systems in high vibration or high-temperature environments, for a fuse to fatigue and fail spontaneously. Such a failure generally will not disco!or the fuse appreciably. If the fuse is replaced and does not blow again, it probably was a random fuse failure. Certain failures, such as the input bridge or one of the chopper transistors, draw such high surge currents that the fuse element will virtually vaporize, and the fuse is noticeably blackened. When this happens, the supply is almost certainly defective and must be repaired. Repeated replacement and blowing of fuses can only increase the damage to the supply.

A malfunctioning EMI filter is isolated by first verifying primary power input, then checking power output at filter connector J31/P31 (fig. 3-1, 3-3).

CAUTION

Use extreme care when handling the core module, It has exposed fine magnet wire which is easily cut. Never remove the core cover. In the event of a core module failure, the module must be returned to the depot for repair.

b. Core Memory. Three circuit modules (Y-driver, X-driver, and 32 kB word array) comprising a core memory are calibrated as a unit at the factory. Although the memory generally operates at room temperature with interchanged boards, its margins may be poor, and malfunctions at extremes of temperature are expected.

Following are guidelines for troubleshooting core memory.

(1) With the control program resident in another module, loop on a failing instruction sequence to isolate the fault to a given memory module. Refer to paragraph 3-12 and the system manual.

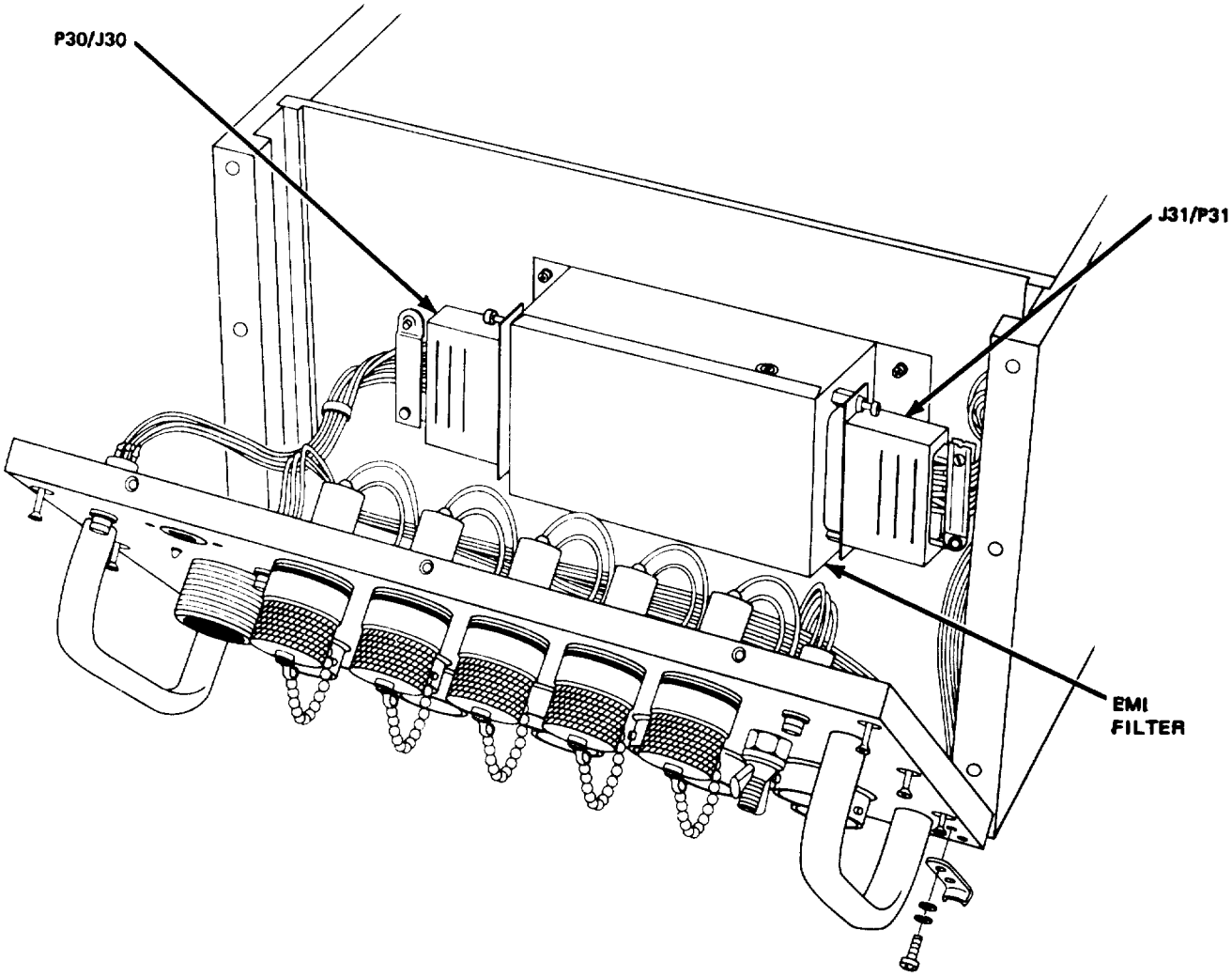


Figure 3-3. EMI Filter and Connectors

(2) If this cannot be done, the defect probably is elsewhere (e.g., memory controller signals, power supply problems, another device on the MEMOUT or MEMIN lines are the wrong time, noise on interface lines, etc.).

CAUTION

Before removing or replacing any of the memory PCBs, make sure the battery back-up supply is disconnected and the primary power source is disconnected or off.

c. Semiconductor Memory. All of the individual semiconductor circuit modules (PCBs) are replaceable and all but the ERCC PCB are interchangeable with like modules. Unlike core memory, the modules are not calibrated as a unit and not subject to the wide and extreme temperature ranges. When interchanging boards, the address selection jumpers must be in the same positions on each board. This enables proper troubleshooting (fault isolation).

d. CPU. CPU repair is not attempted in the field. Failed CPU boards are sent to the special repair activity (SRA) facility for repair.

3-7. USE OF TROUBLESHOOTING FLOWCHARTS

a. Locate the malfunction in the sympton index on page 3-14.

b. Note that the troubleshooting flowcharts and procedures are indexed by malfunction/symptom.

c. Review the sample flowchart (fig. 3-4) to become familiar with the proper use of troubleshooting flowcharts.

3-8. SYMPTOM INDEX

Table 3-5 provides an index of probable equipment malfunction symptoms. Use the index to quickly locate applicable troubleshooting flowchart and/or procedures to determine the required corrective action(s).

3-9. TROUBLESHOOTING PROCEDURES

The paragraphs to follow define the proper and approved approach to troubleshooting the processor. Maintenance technicians working on the processor will find that using this troubleshooting approach, in conjunction with the information already supplied in paragraphs 3-6 through 3-8, ensures rapid and accurate identification of malfunctions within the unit. Although some of the troubleshooting tasks discussed are tasks not performed by direct support maintenance personnel, having already been performed by organizational maintenance or to be performed by general support, the SRA, or depot personnel, it is to the direct support maintenance technician's advantage to be aware of the entire troubleshooting process.

The first step in servicing a defective processor is to trace the fault to an assembly or subassembly within the processor (e.g., power supply, printed circuit board, etc.). This is

called SECTIONALIZATION, which is accomplished by conducting checks and operational tests. These checks and tests help determine the exact nature of the fault.

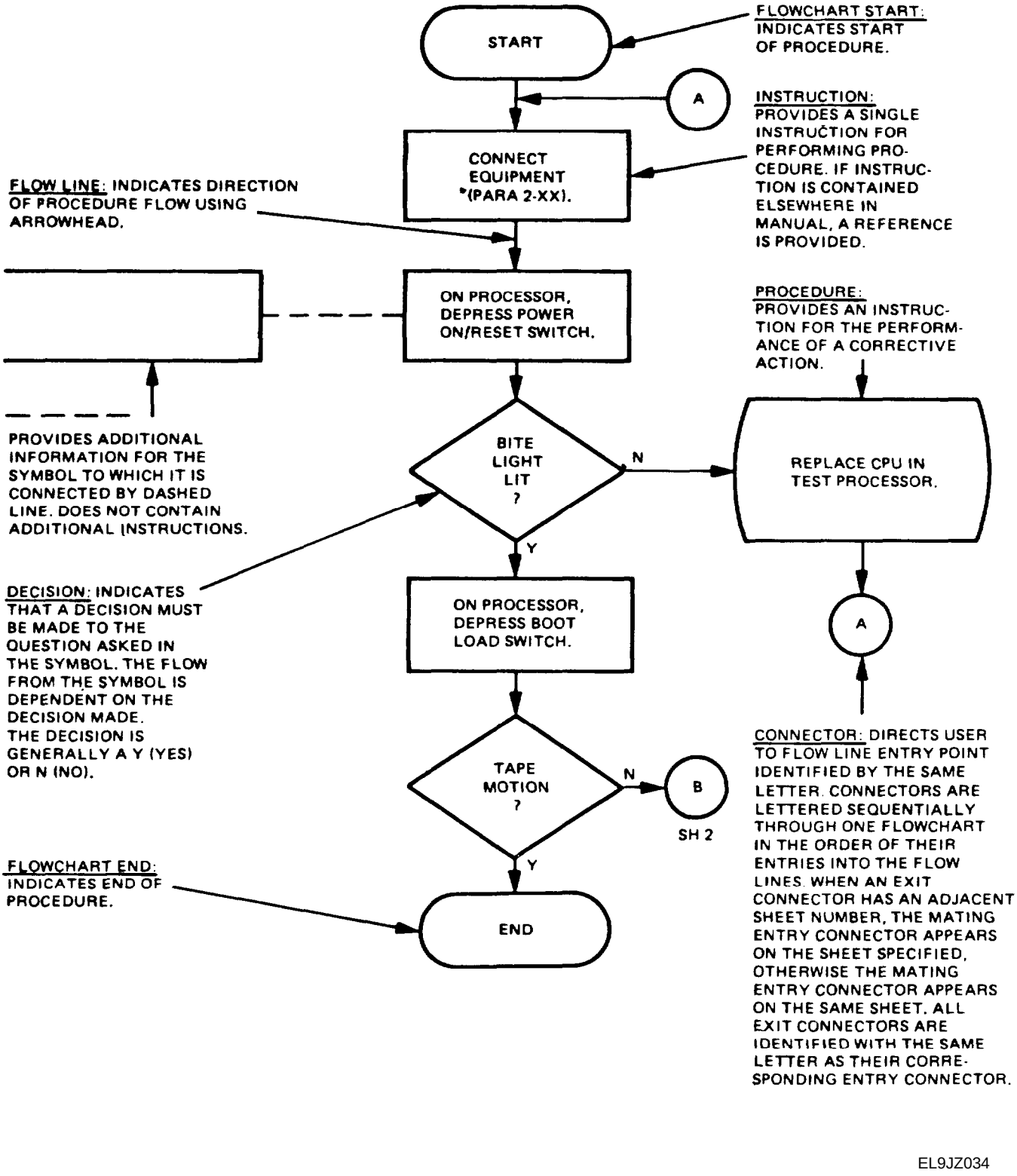


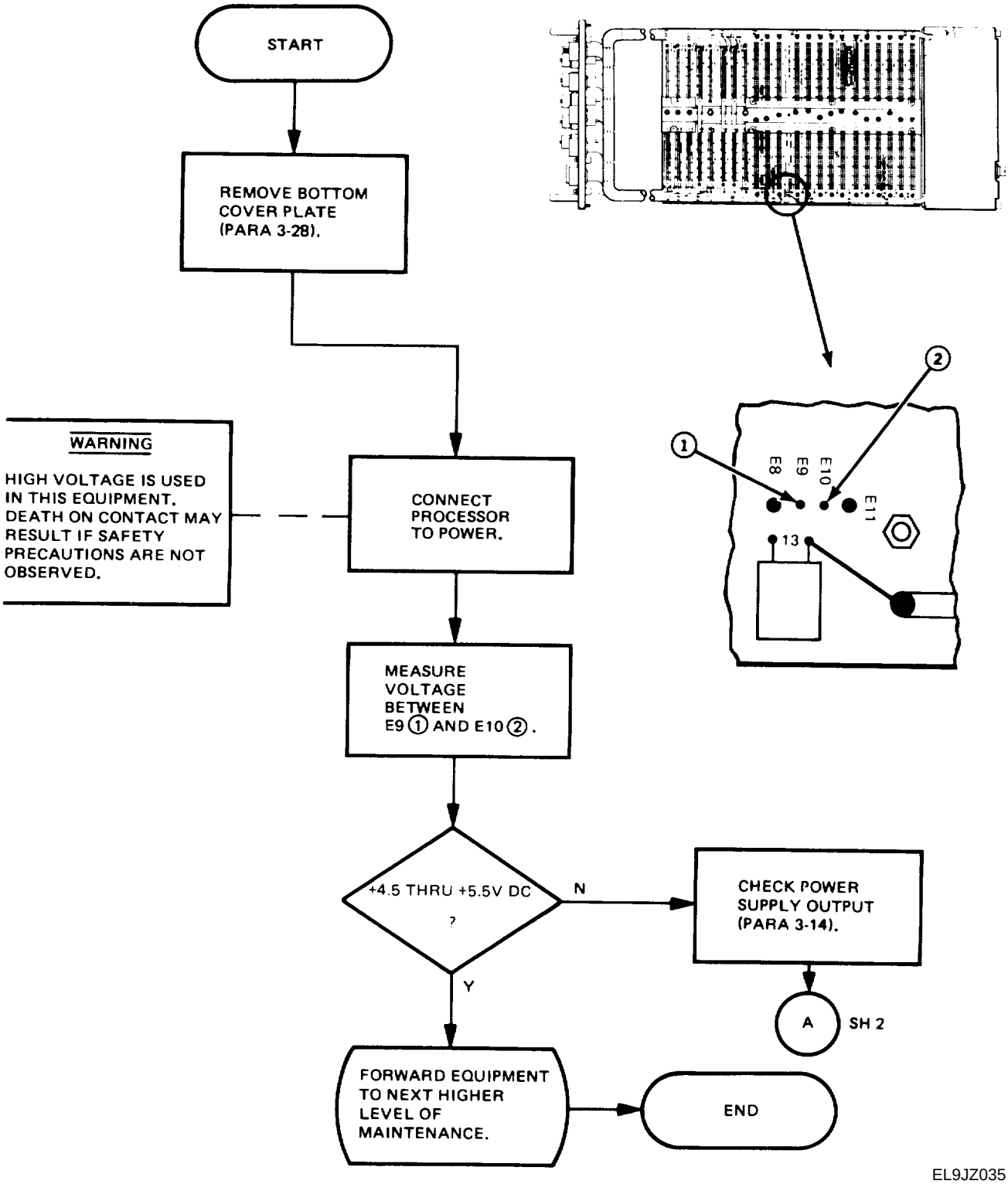
Figure 3-4. How to Use the Flowchart, Sample Flowchart

Table 3-5. Processor Malfunction/Symptom Index

Malfunction/Symptom	Flowchart Para Number
1. Smoke and fire.	Para 3-9a
2. Unit overheating.	Para 3-9b
3. Noisy blower fan.	Para 3-9c
4. PWR ON/RESET, BITE/BOOT, BAIT indicators not lit.	Flowchart
5. PWR ON/RESET indicator not lit (core memory).	Flowchart
6. PWR ON/RESET indicator not lit. (semi memory).	Flowchart
7. BITE/BOOT indicator not lit (core memory).	Flowchart
8. BITE/BOOT indicator not lit (semi memory).	Flowchart
9. BATT indicator not lit.	Flowchart
10. RUN/RESET indicator won't light (core memory).	Flowchart
11. RUN/RESET indicator won't light (semi memory).	Flowchart
12. Defective ETM indicator.	Para 3-9g
13. Program won't load.	Para 3-9h
14. Processor does not accept data.	Para 3-9i
15. Processor does not output data.	Para 3-9j
16. Processor keeps blowing fuses.	Flowchart

TROUBLESHOOTING FLOWCHART 1

PWR ON/RESET, BITE/BOOT, BATT INDICATORS NOT LIT (SHEET 1 OF 2)



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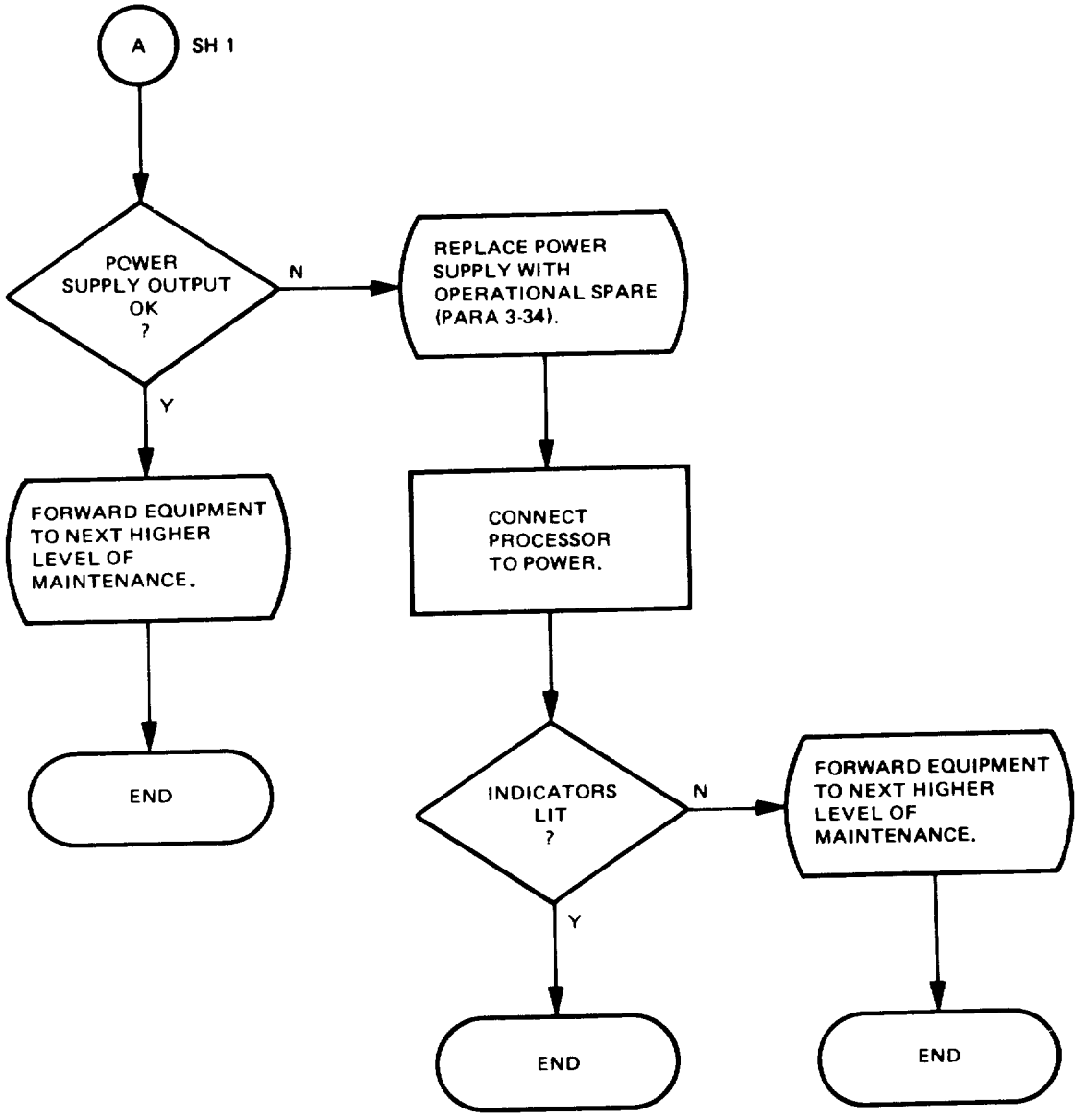
TROUBLESHOOTING FLOWCHART 1

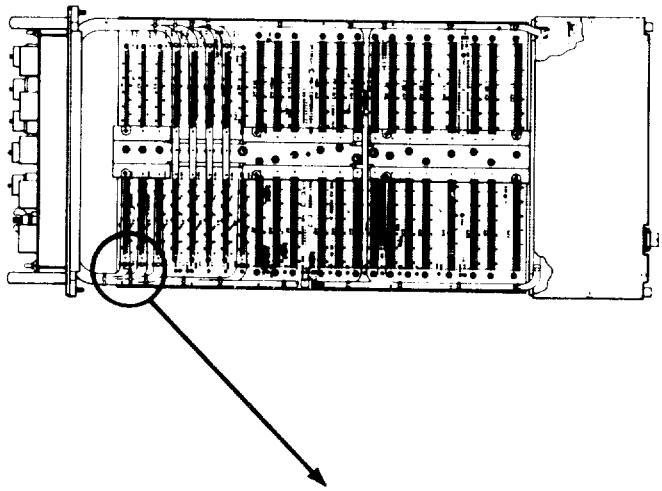
PWR ON/RESET, BITE/BOOT, BATT INDICATORS NOT LIT (SHEET 2 OF 2)



EL9JZ036

TROUBLESHOOTING FLOWCHART 2

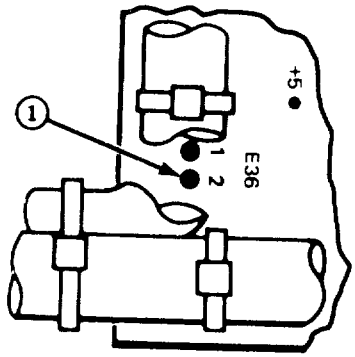
PWR ON/RESET INDICATOR NOT LIT, CORE MEMORY (SHEET 1 OF 14)



START

REMOVE FRONT PANEL (PARA 3-30).

REMOVE BOTTOM COVER PLATE (PARA 3-28).



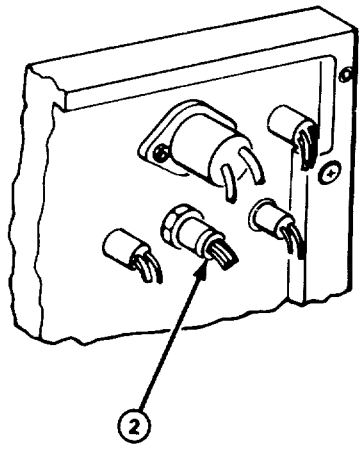
WARNING

HIGH VOLTAGE IS USED IN THIS EQUIPMENT. DEATH ON CONTACT MAY RESULT IF SAFETY PRECAUTIONS ARE NOT OBSERVED.

CONNECT PROCESSOR TO POWER.

E36-2 IS POSITIVE.

CHECK VOLTAGE BETWEEN E36-2 (1) AND E60 (2).

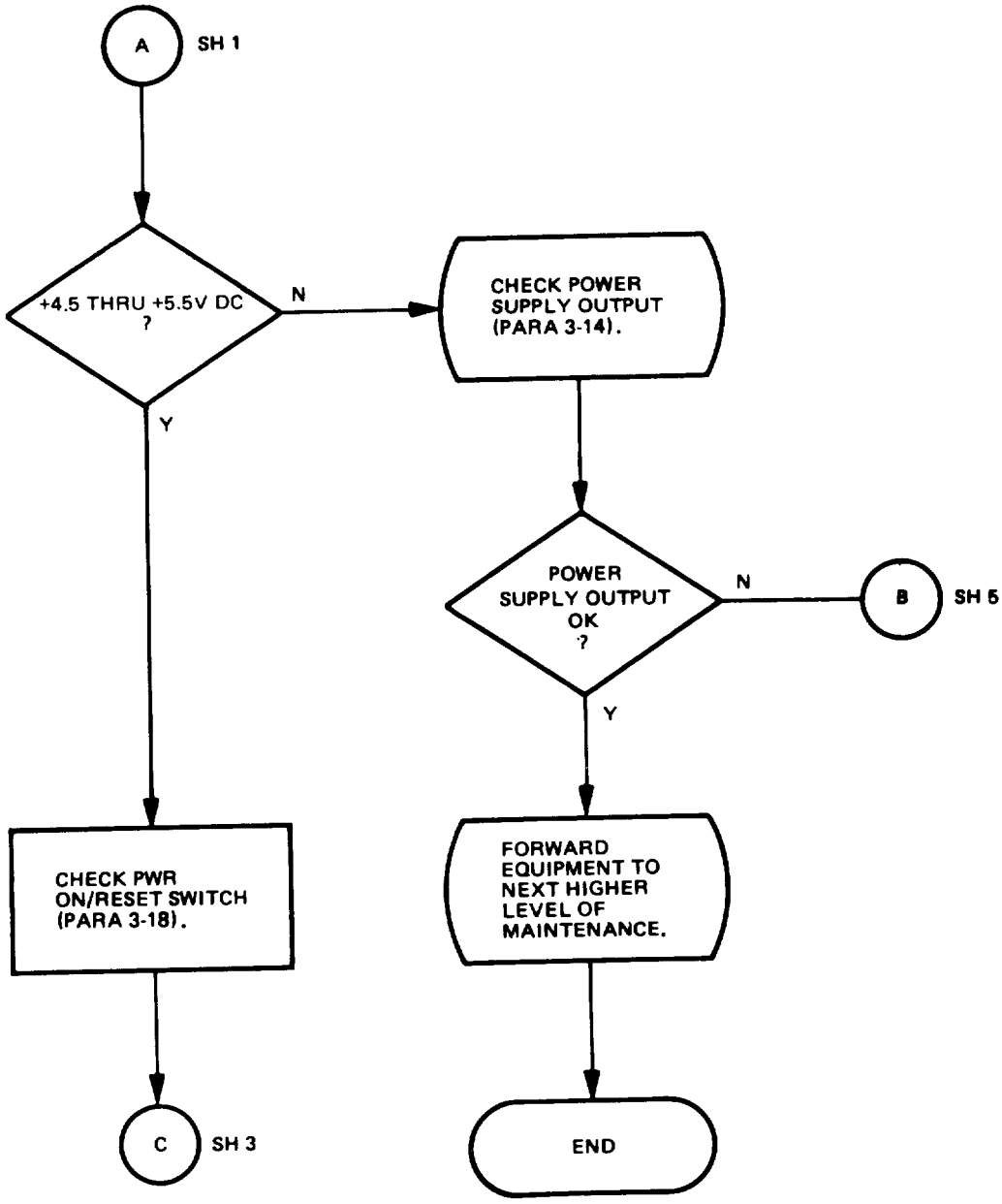


A SH 2

EL9JZ037

TROUBLESHOOTING FLOWCHART 2

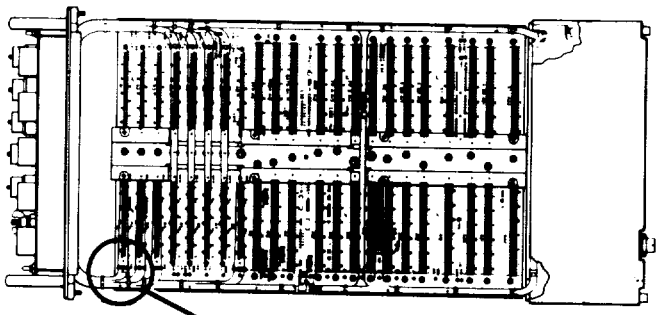
PWR ON/RESET INDICATOR NOT LIT, CORE MEMORY (SHEET 2 OF 14)

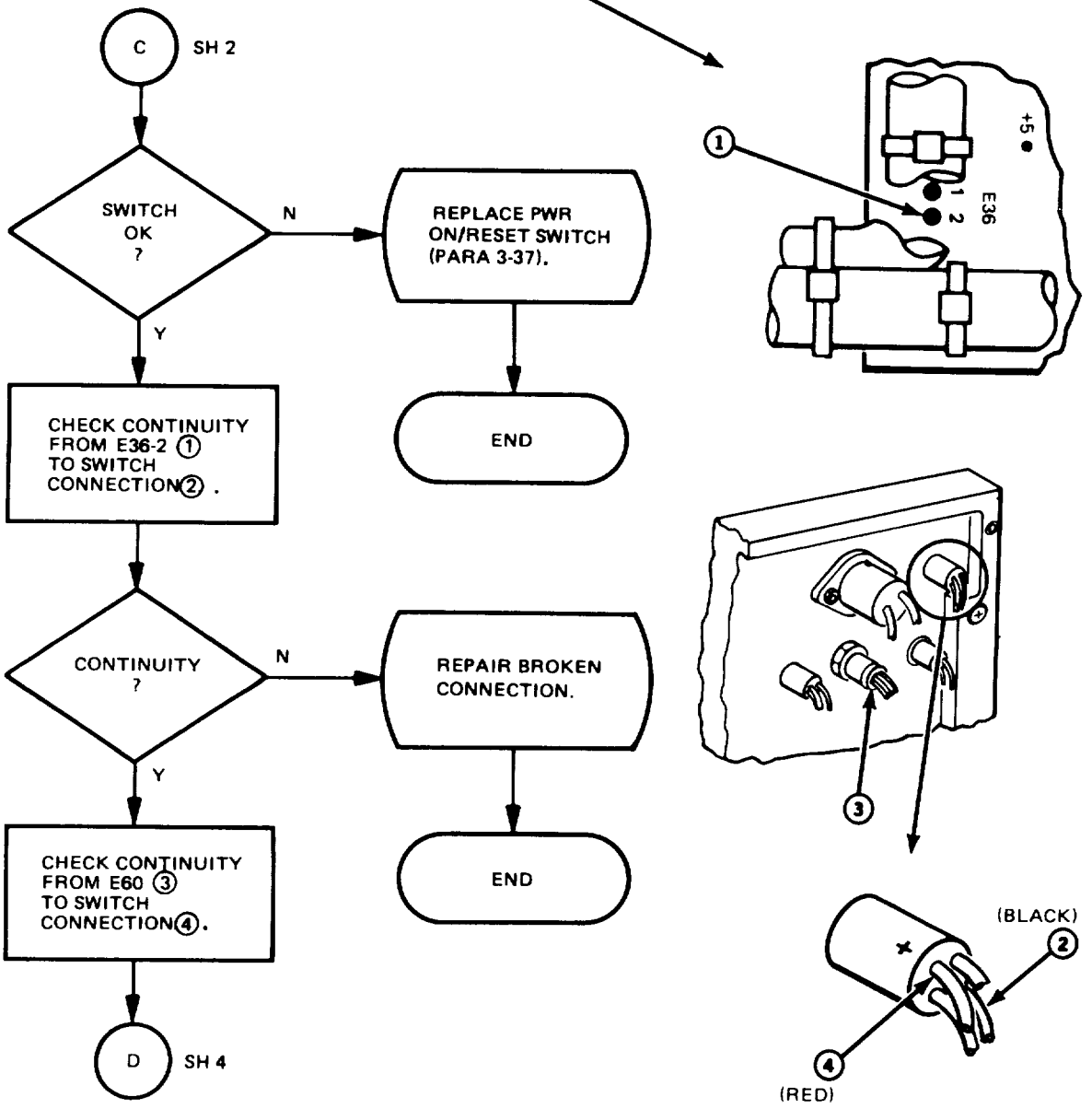


EL9JZ038

TROUBLESHOOTING FLOWCHART 2

PWR ON/RESET INDICATOR NOT LIT, CORE MEMORY (SHEET 3 OF 14)

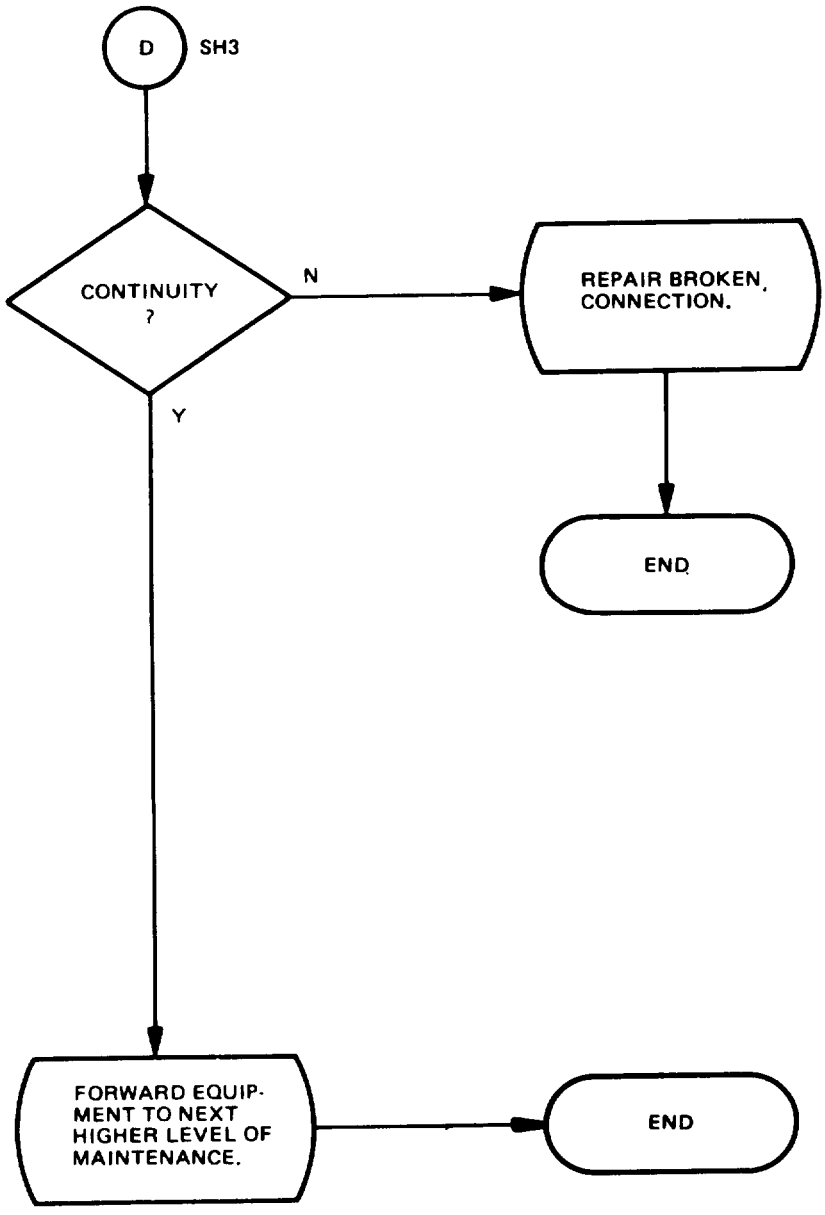




EL9JZ039

TROUBLESHOOTING FLOWCHART 2

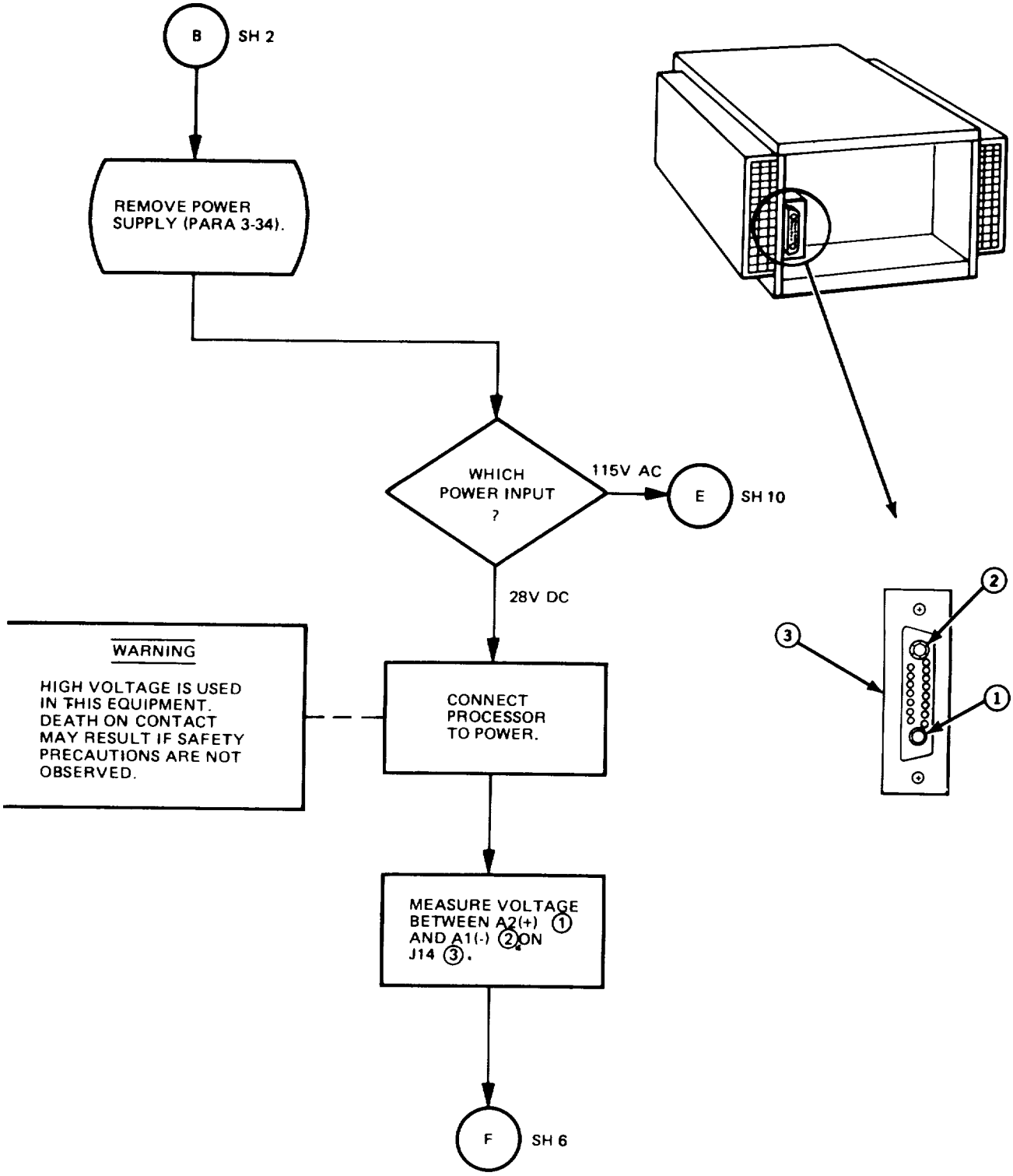
PWR ON/RESET INDICATOR NOT LIT, CORE MEMORY (SHEET 4 OF 14)



EL9JZM0

TROUBLESHOOTING FLOWCHART 2

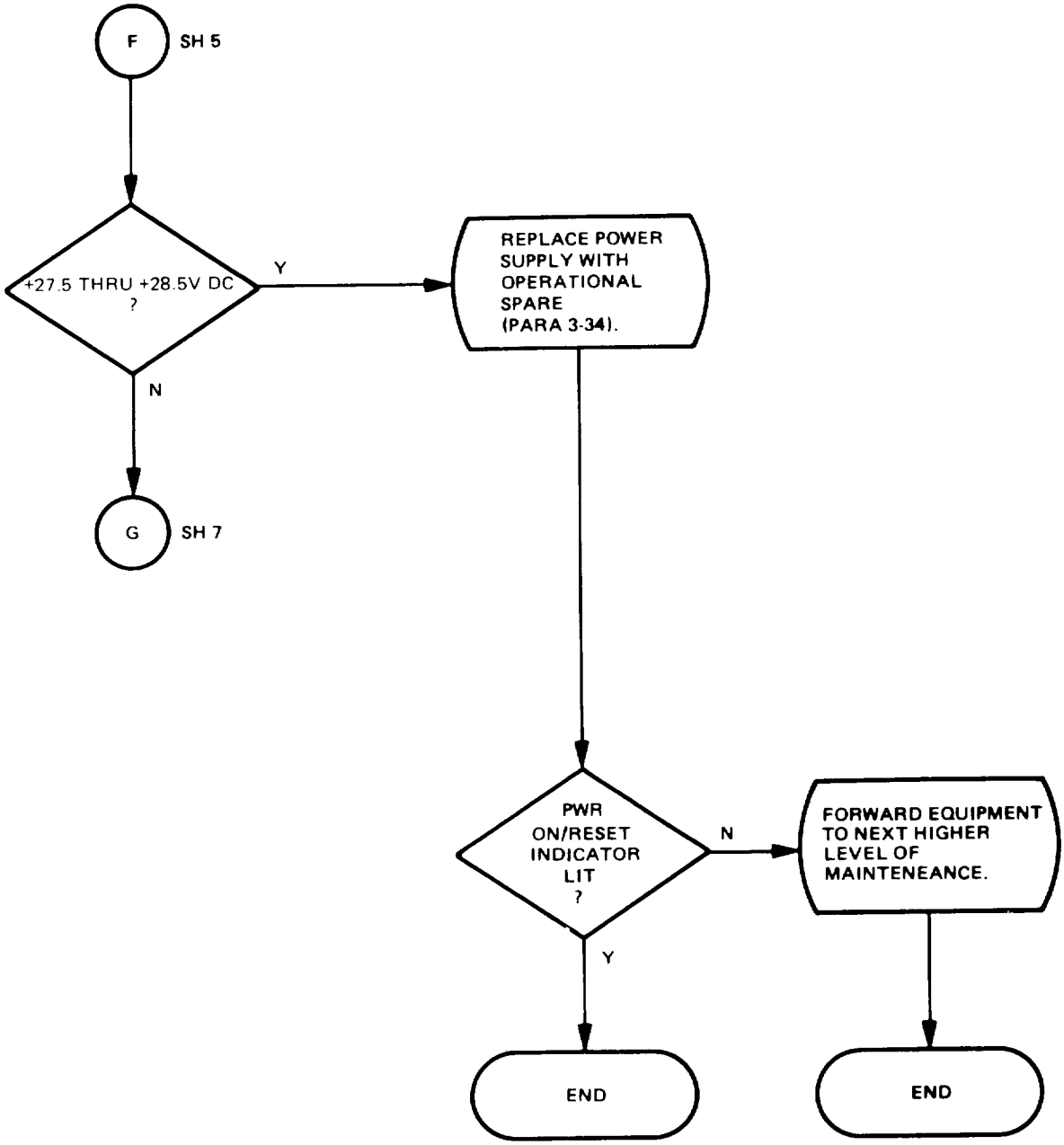
PWR ON/RESET INDICATOR NOT LIT, CORE MEMORY (SHEET 5 OF 14)



EL9JZ041

TROUBLESHOOTING FLOWCHART 2

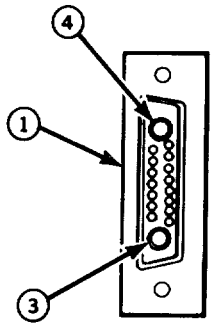
PWR ON/RESET INDICATOR NOT LIT, CORE MEMORY (SHEET 6 OF 14)

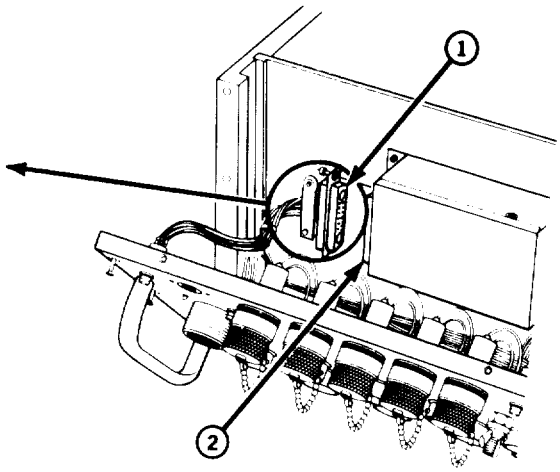


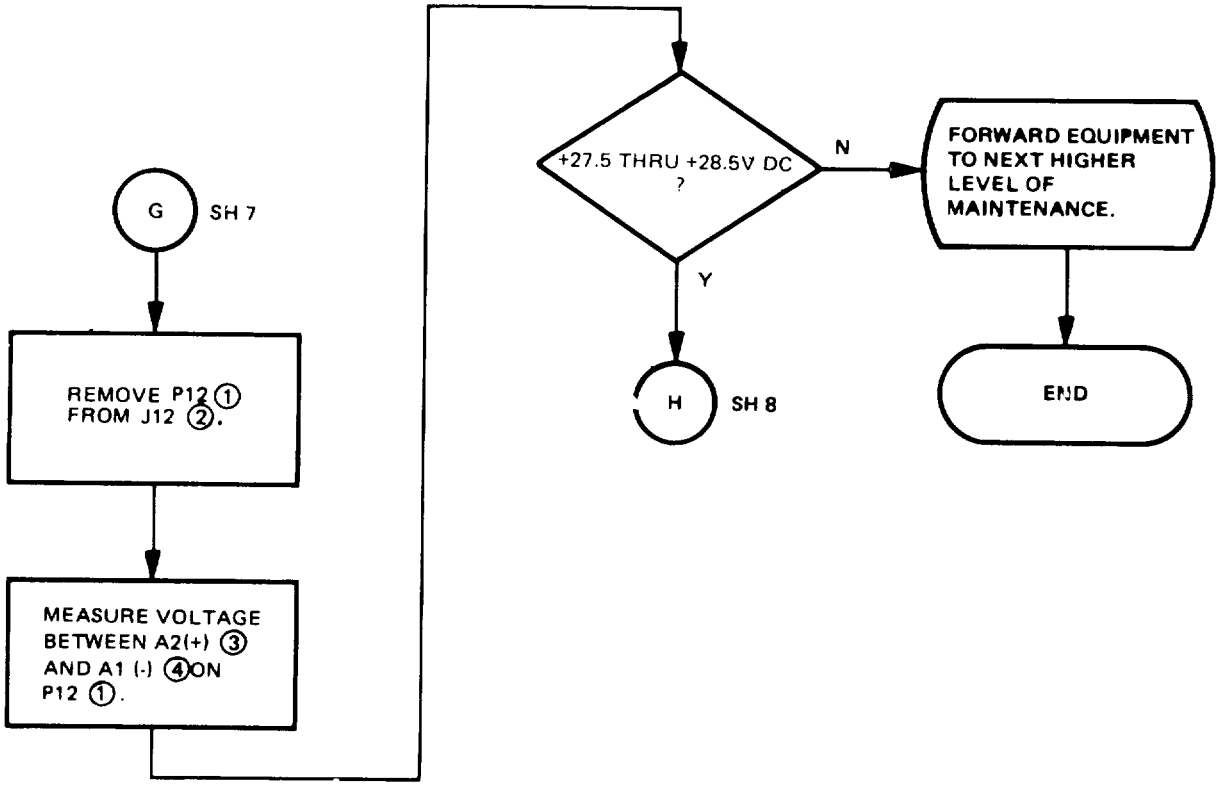
EL9JZ042

TROUBLESHOOTING FLOWCHART 2

PWR ON/RESET INDICATOR NOT LIT, CORE MEMORY (SHEET 7 OF 14)



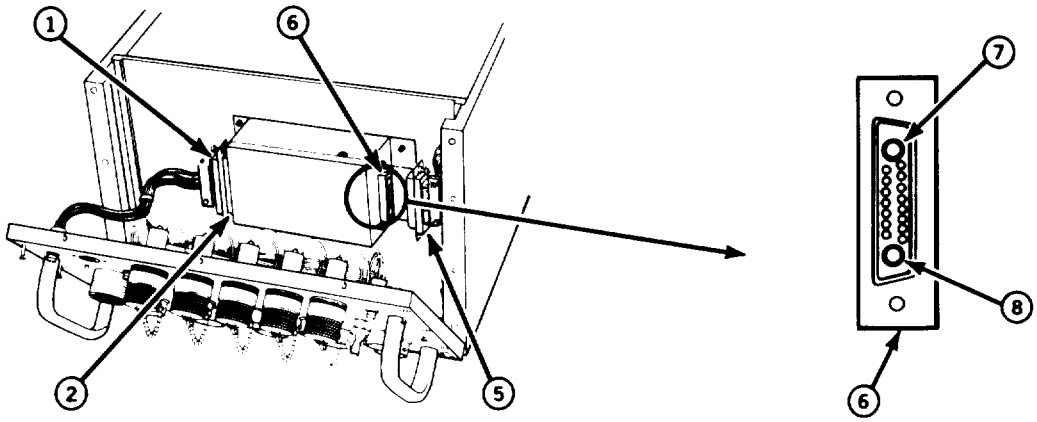


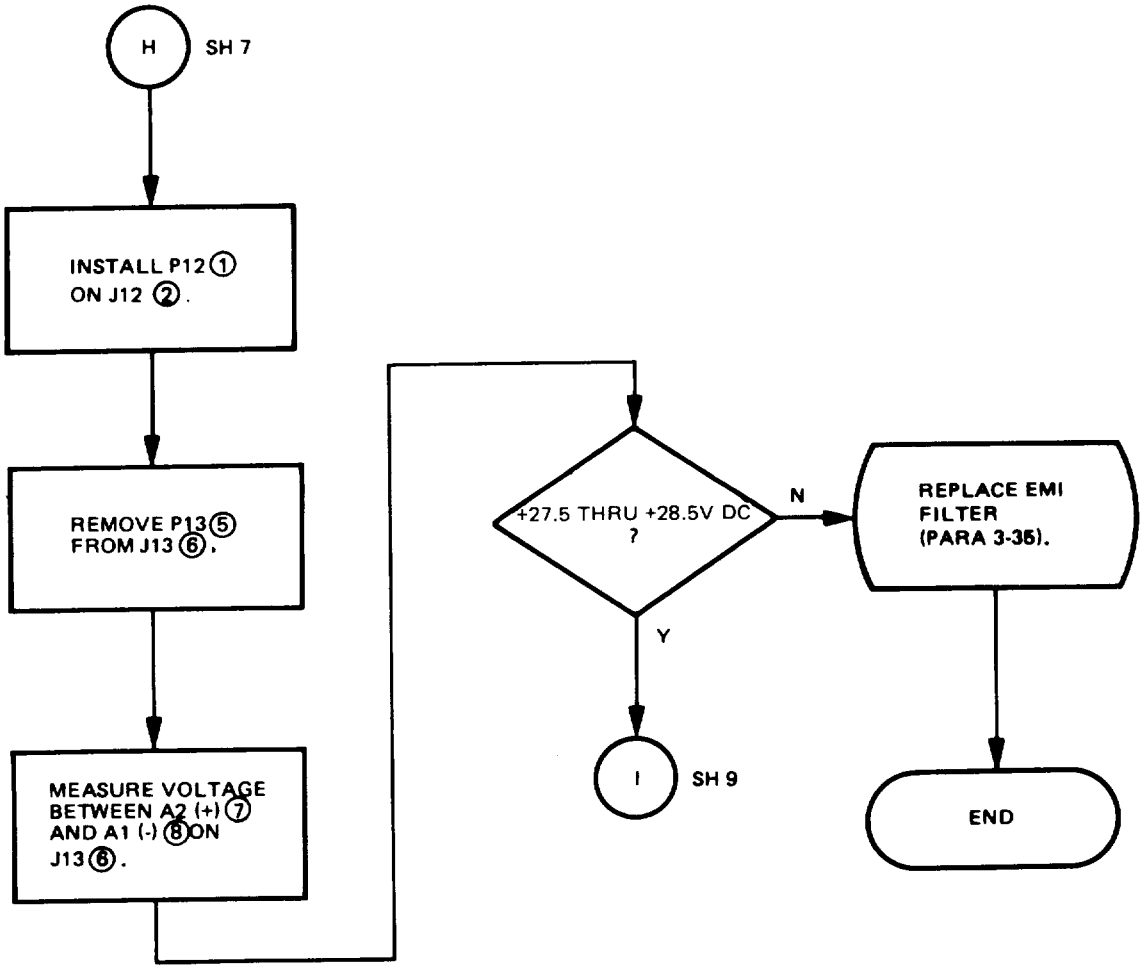


EL9JZ043

TROUBLESHOOTING FLOWCHART 2

PWR ON/RESET INDICATOR NOT LIT, CORE MEMORY (SHEET 8 OF 14)

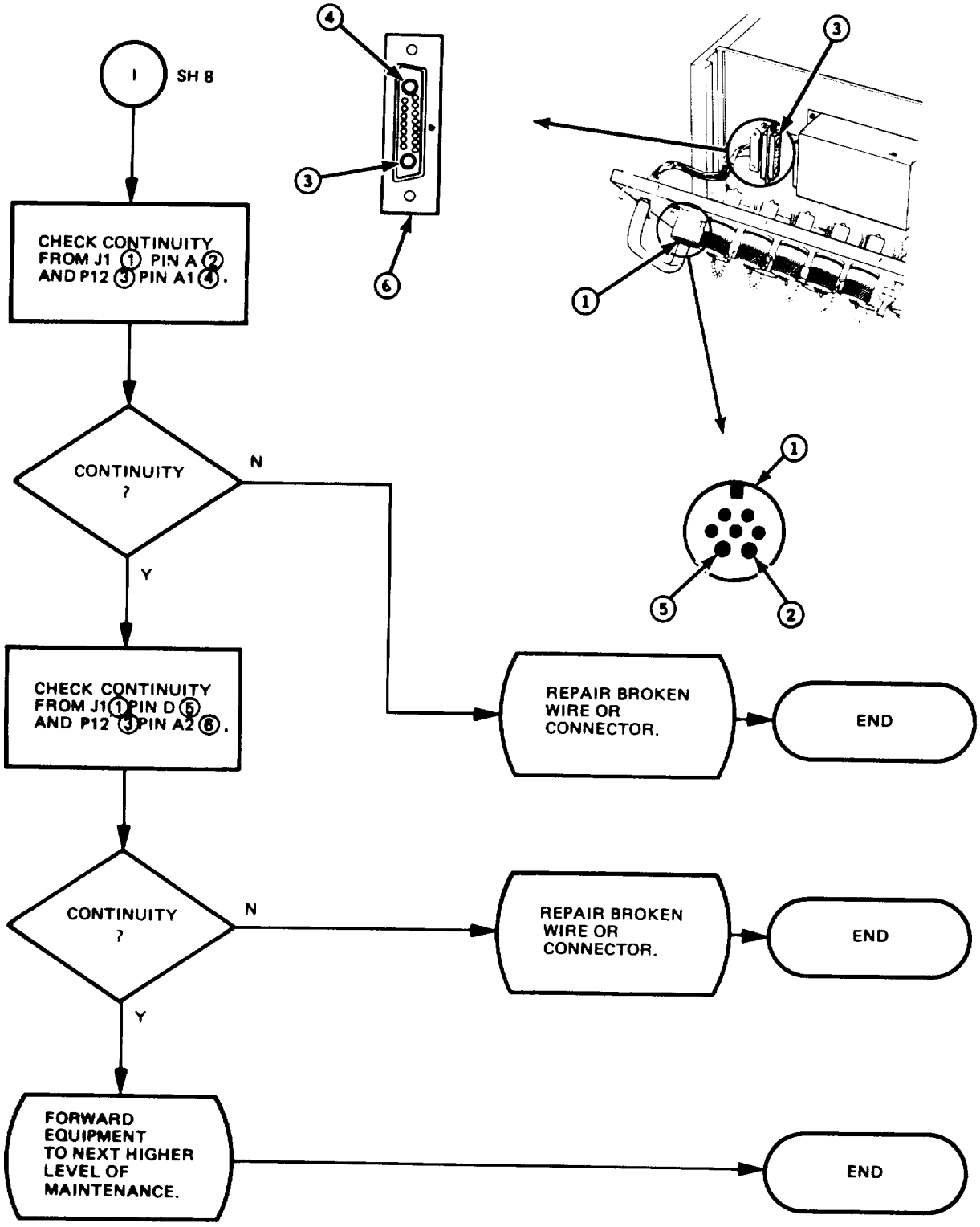




EL9JZ044

TROUBLESHOOTING FLOWCHART 2

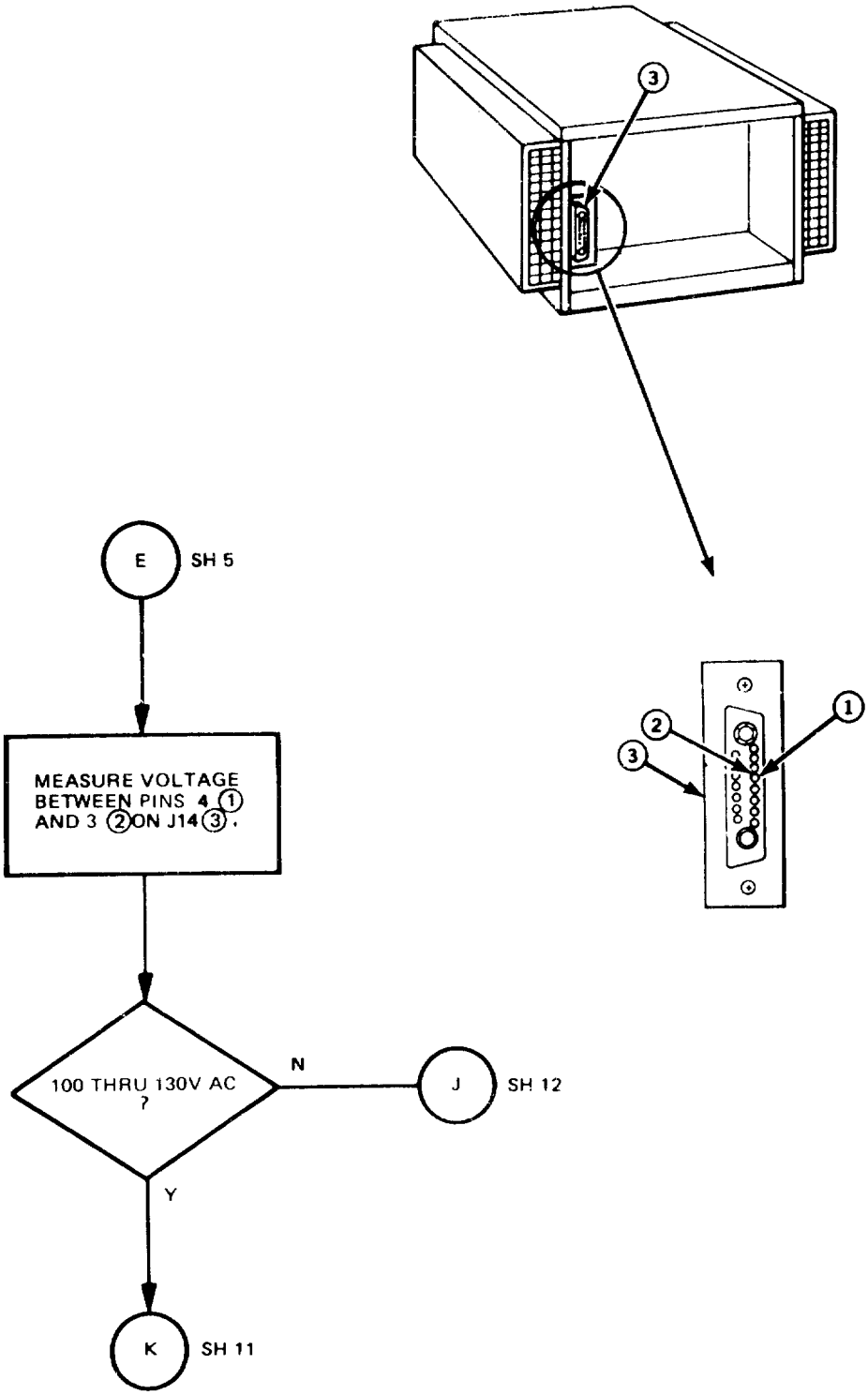
PWR ON/RESET INDICATOR NOT LIT, CORE MEMORY (SHEET 9 OF 14)



EL9JZ045

TROUBLESHOOTING FLOWCHART 2

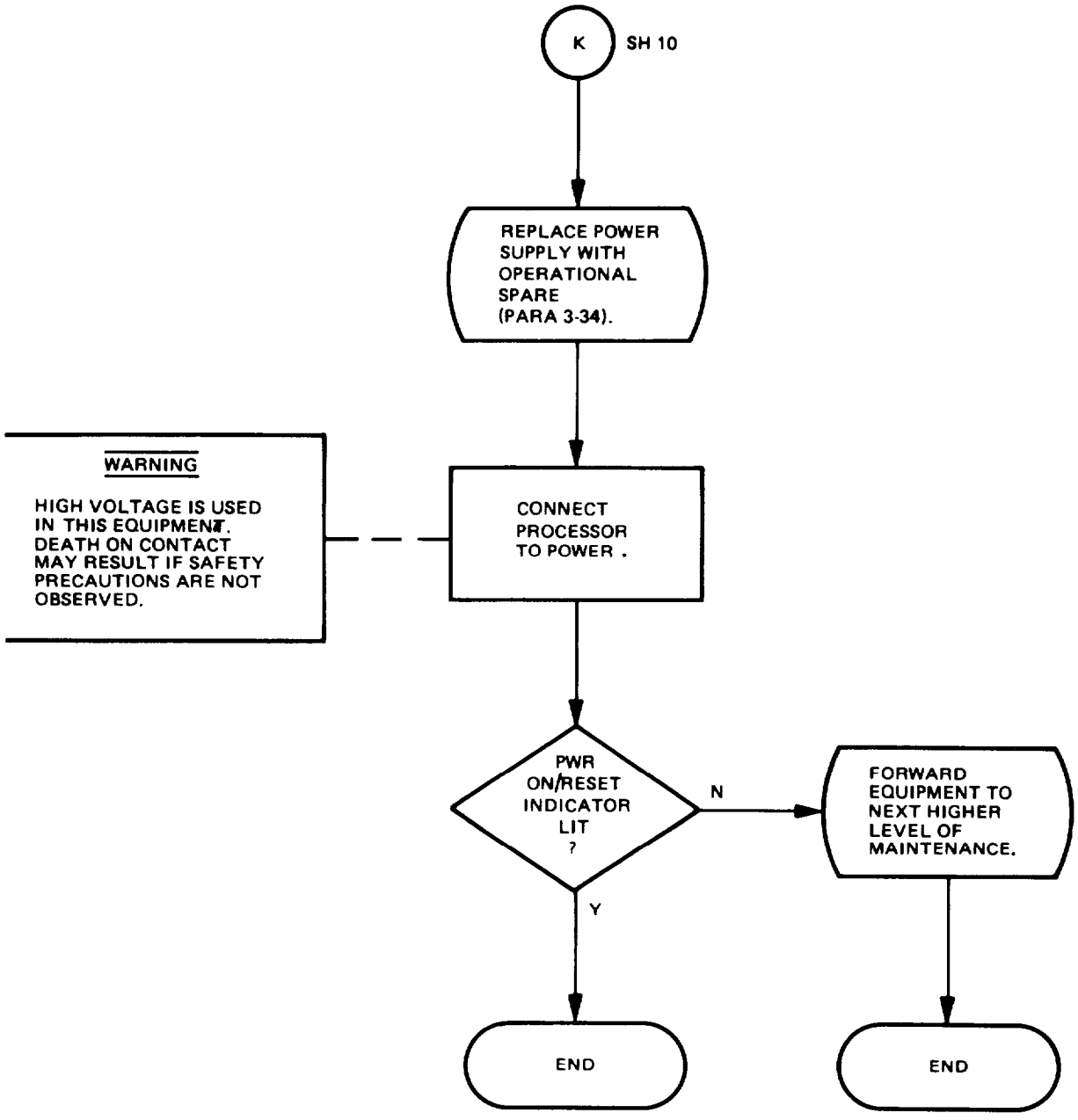
PWR ON/RESET INDICATOR NOT LIT, CORE MEMORY (SHEET 10 OF 14)



EL9JZ046

TROUBLESHOOTING FLOWCHART 2

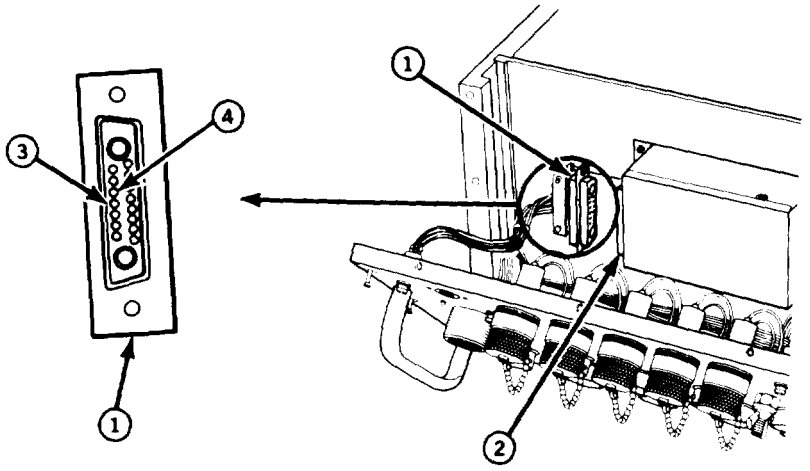
PWR ON/RESET INDICATOR NOT LIT, CORE MEMORY (SHEET 11 OF 14)

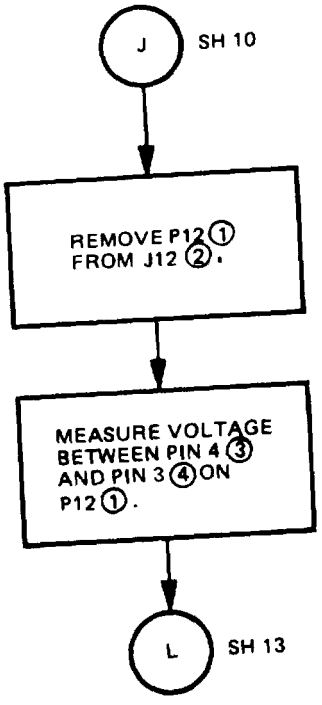


EL9JZ047

TROUBLESHOOTING FLOWCHART 2

PWR ON/RESET INDICATOR NOT LIT, CORE MEMORY (SHEET 12 OF 14)

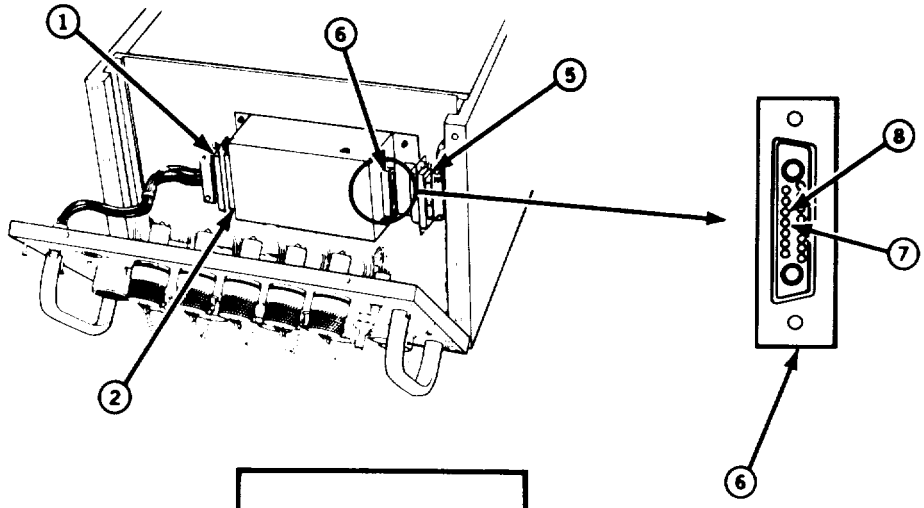


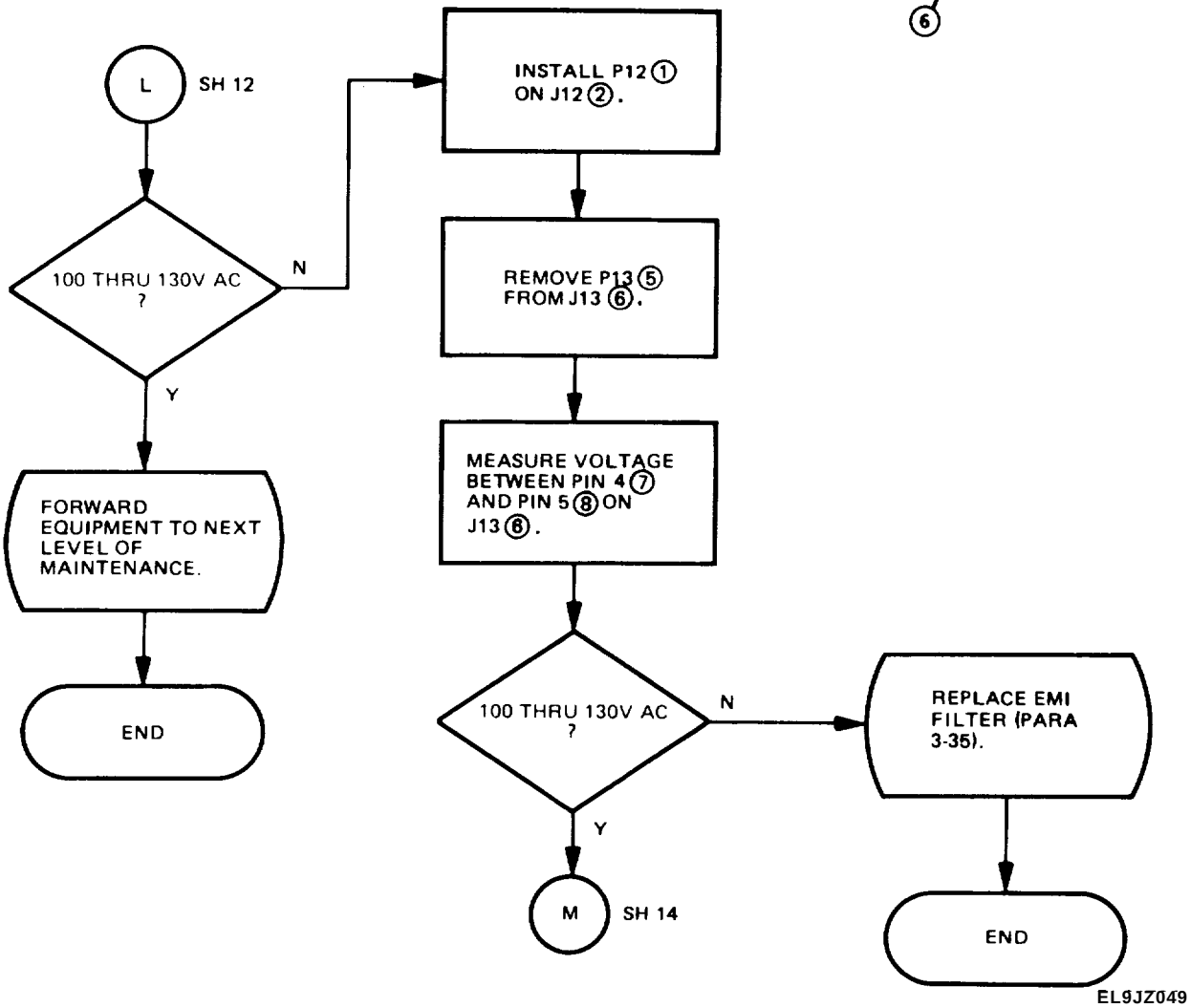


EL9JZ048

TROUBLESHOOTING FLOWCHART 2

PWR ON/RESET INDICATOR NOT LIT, CORE MEMORY (SHEET 13 OF 14)

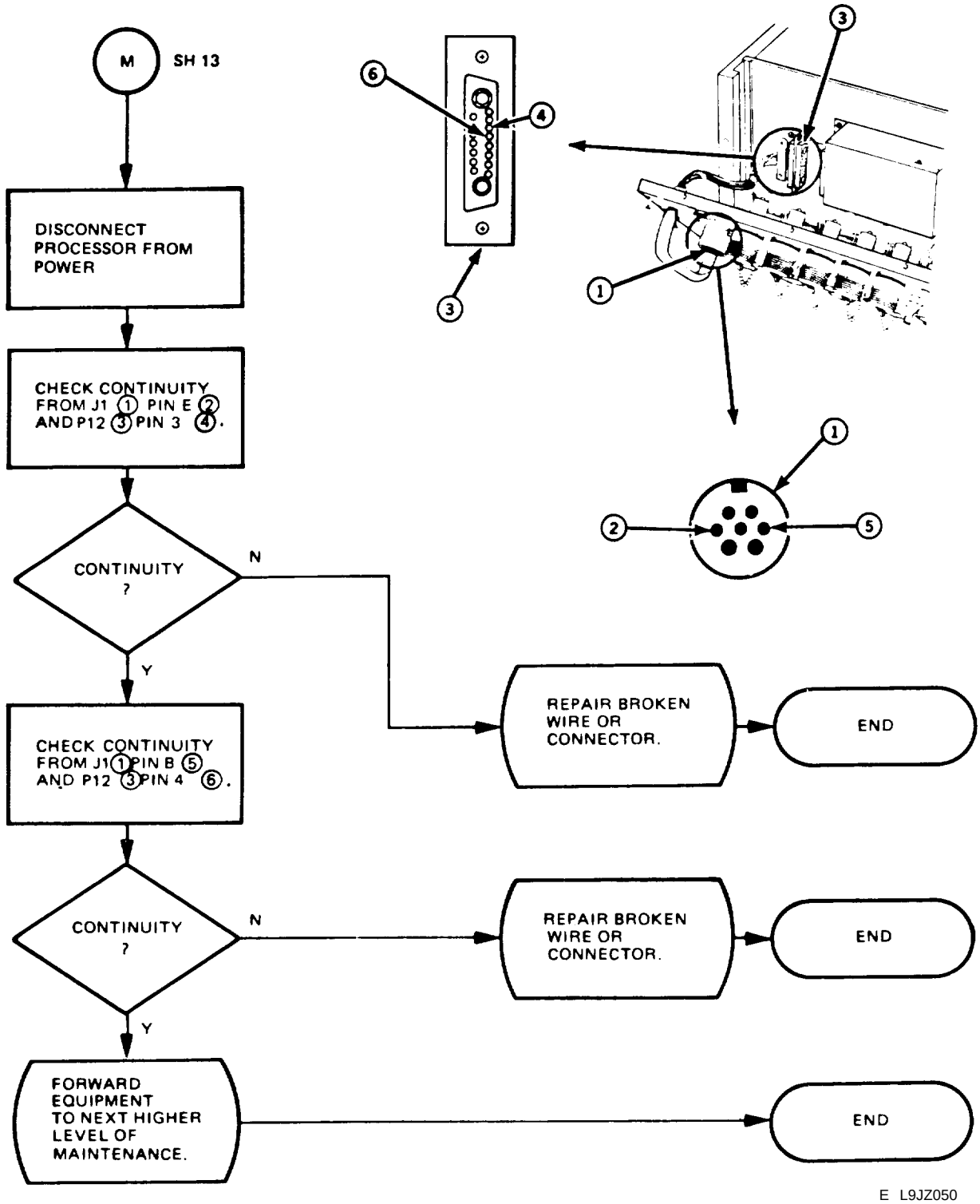




EL9JZ049

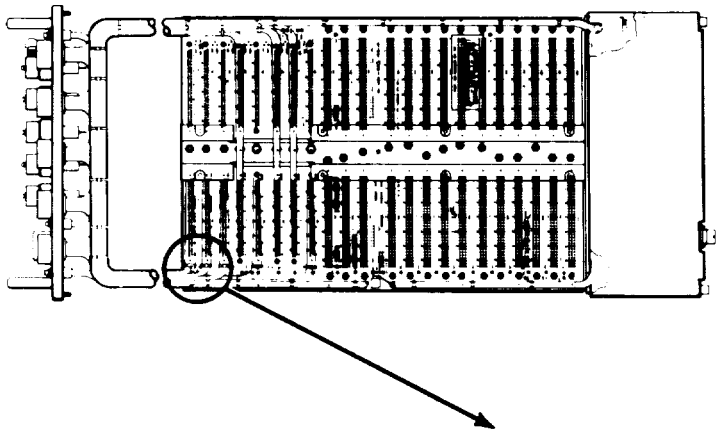
TROUBLESHOOTING FLOWCHART 2

PWR ON/RESET INDICATOR NOT LIT, CORE MEMORY (SHEET 14 OF 14)



TROUBLESHOOTING FLOWCHART 3

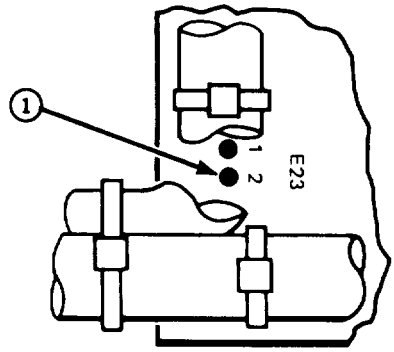
PWR ON/RESET INDICATOR NOT LIT, SEMI MEMORY (SHEET 1 OF 14)



START

REMOVE FRONT PANEL (PARA 3-30).

REMOVE BOTTOM COVER PLATE (PARA 3-28).



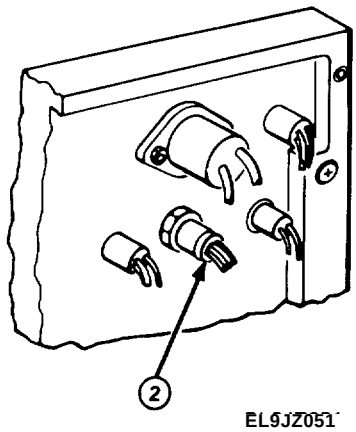
WARNING

HIGH VOLTAGE IS USED IN THIS EQUIPMENT. DEATH ON CONTACT MAY RESULT IF SAFETY PRECAUTIONS ARE NOT OBSERVED.

CONNECT PROCESSOR TO POWER.

E23-2 IS POSITIVE.

CHECK VOLTAGE BETWEEN E23-2 (1) AND E60 (2).

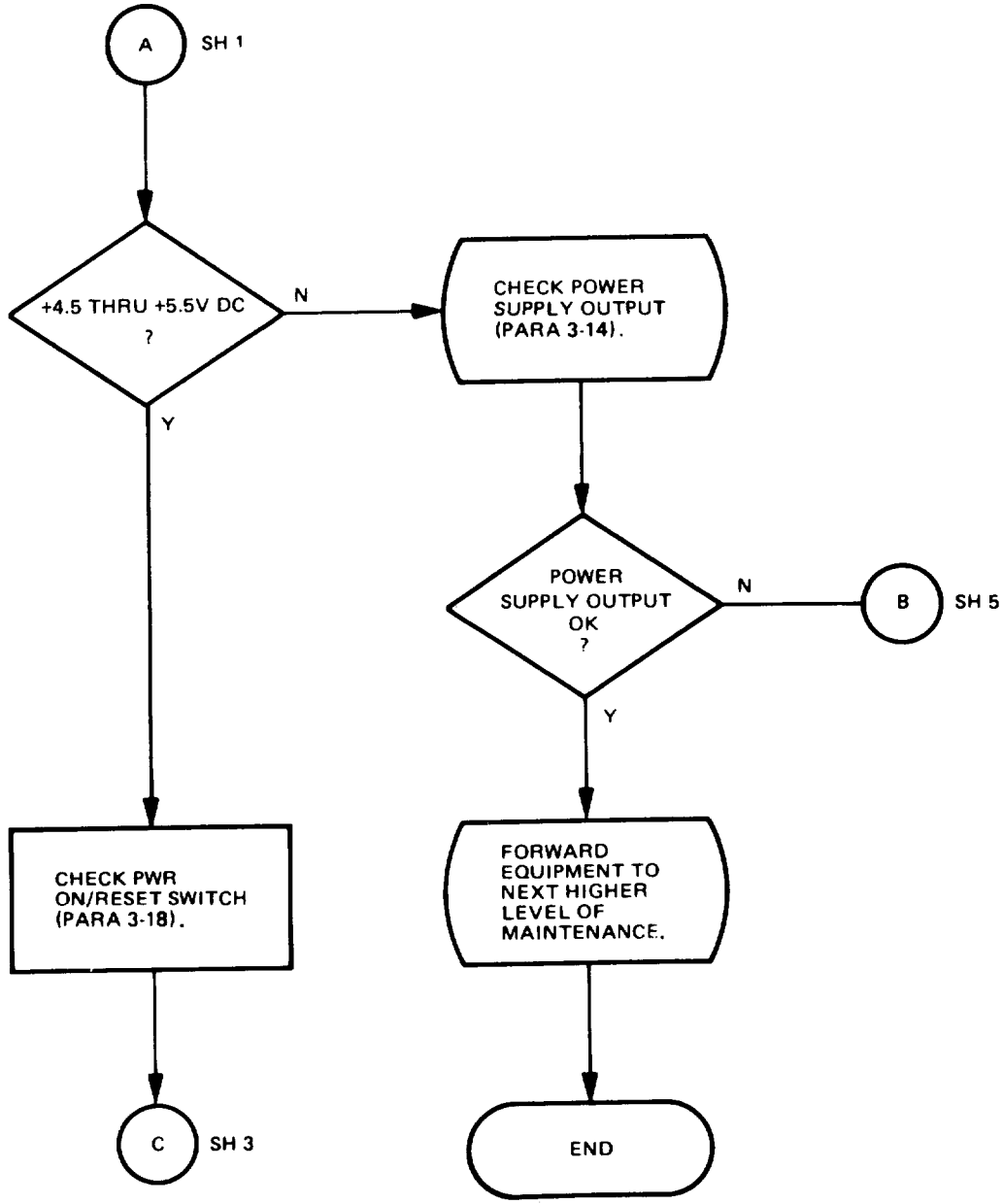


A SH 2

EL9JZ051

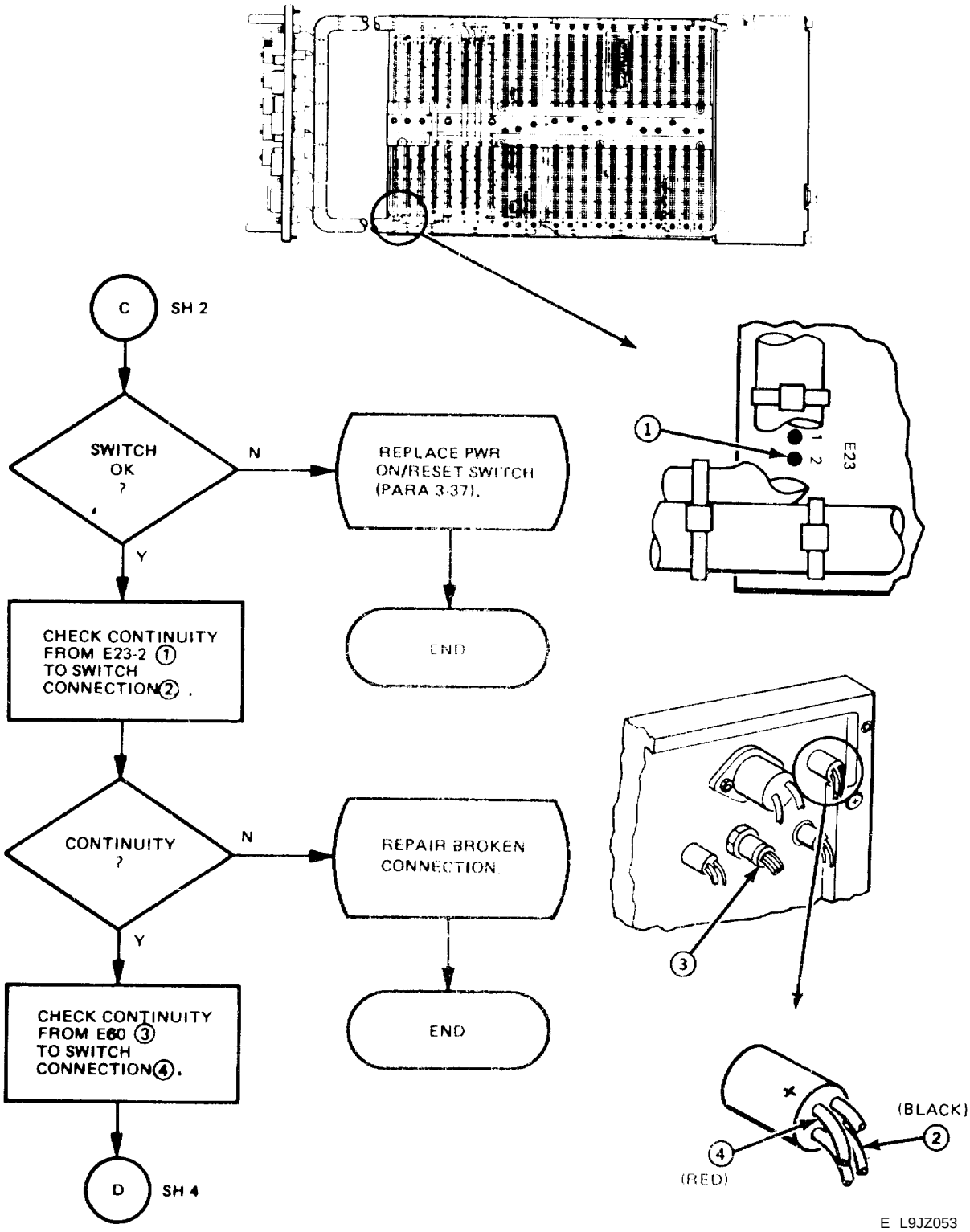
TROUBLESHOOTING FLOWCHART 3

PWR ON/RESET INDICATOR NOT LIT, SEMI MEMORY (SHEET 2 OF 14)



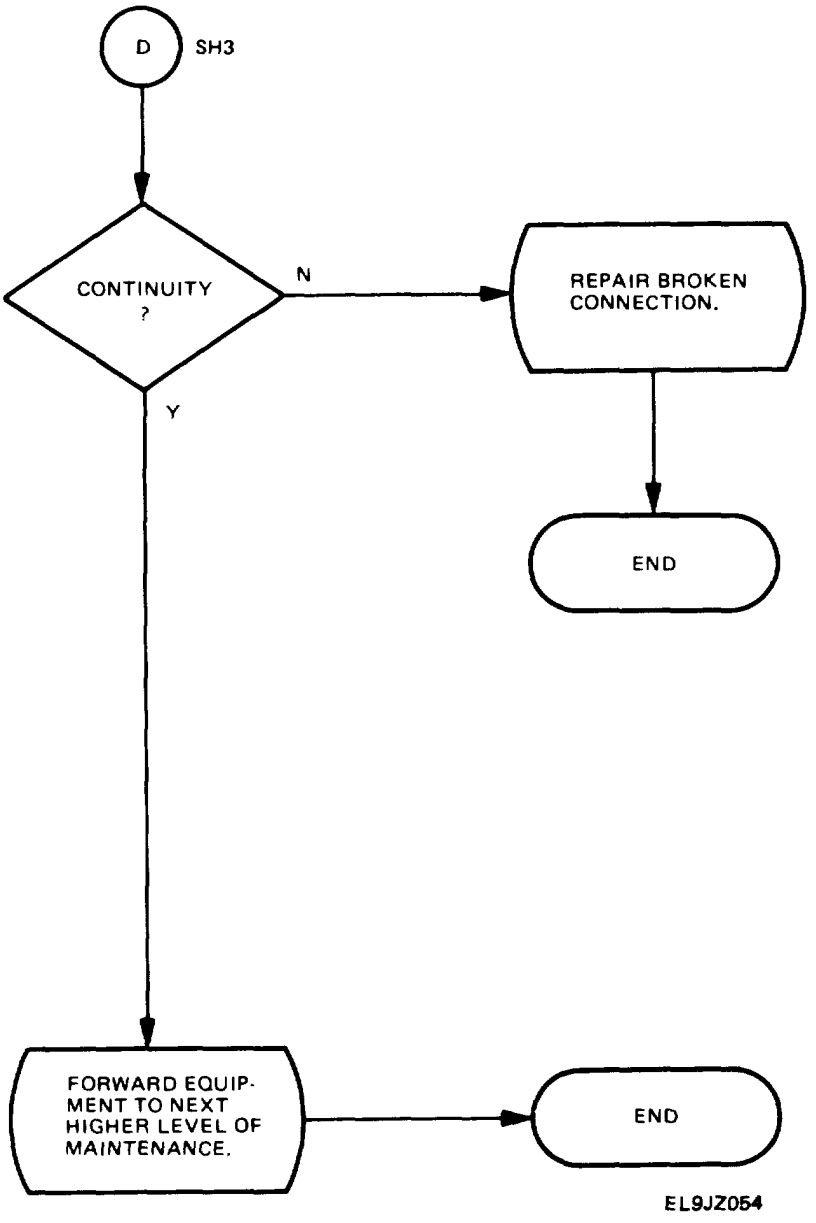
TROUBLESHOOTING FLOWCHART 3

PWR ON/RESET INDICATOR NOT LIT, SEMI MEMORY (SHEET 3 OF 14)



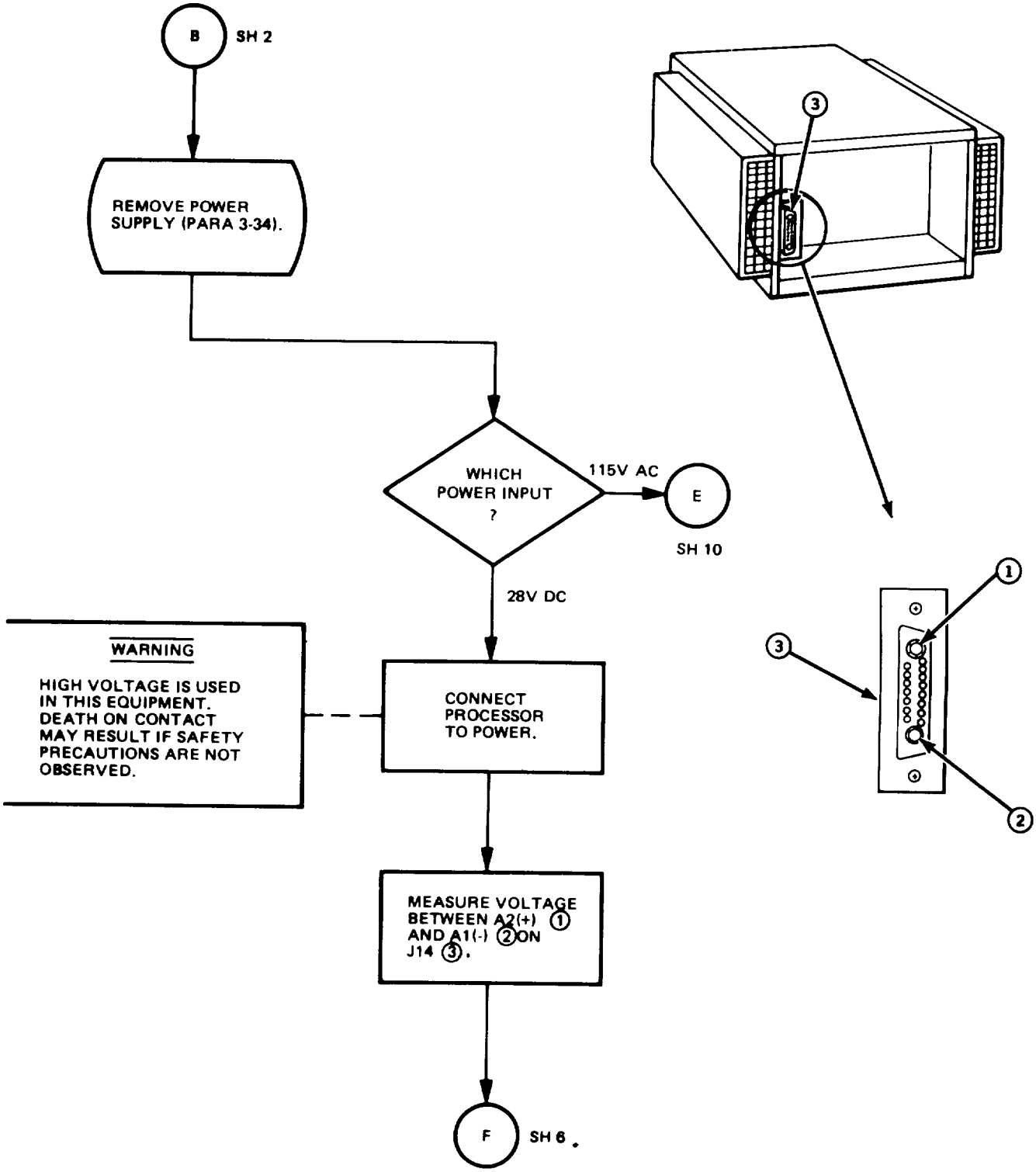
TROUBLESHOOTING FLOWCHART 3

PWR ON/RESET INDICATOR NOT LIT, SEMI MEMORY (SHEET 4 OF 14)



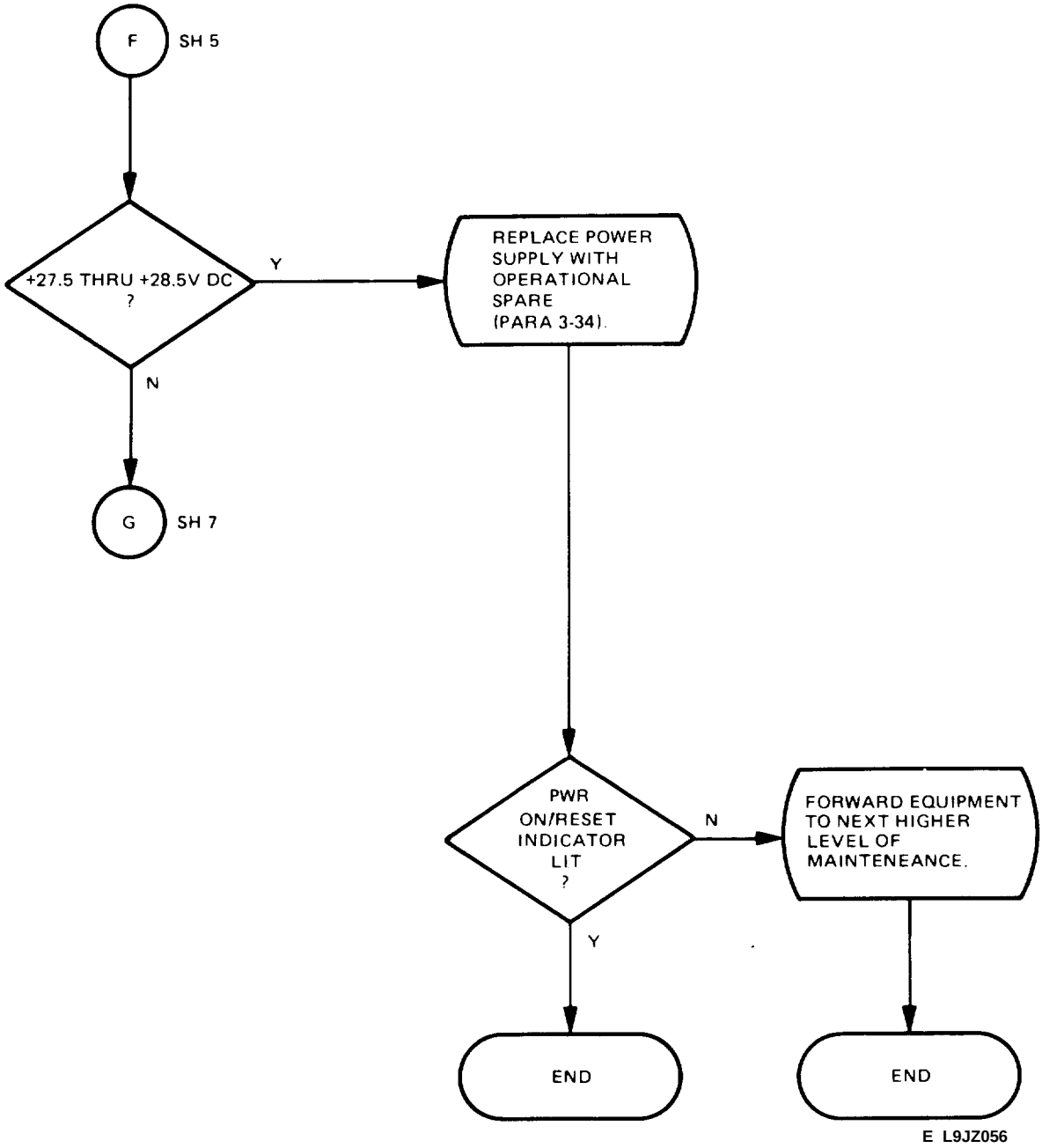
TROUBLESHOOTING FLOWCHART 3

PWR ON/RESET INDICATOR NOT LIT, SEMI MEMORY (SHEET 5 OF 14)



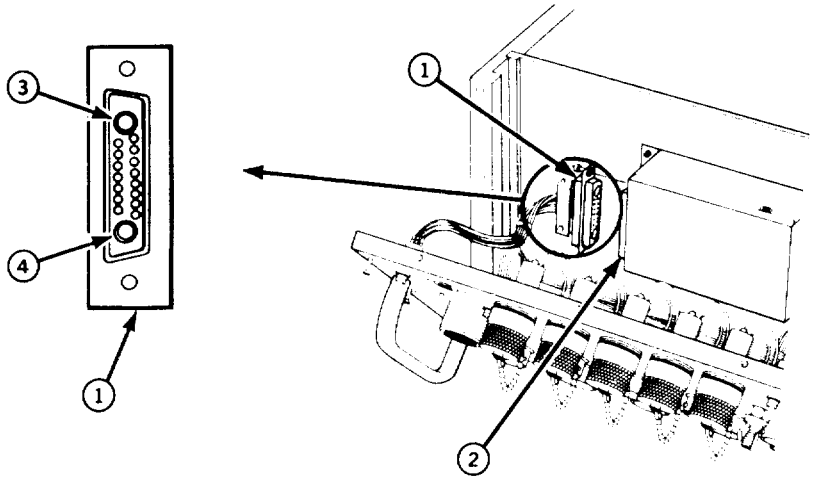
TROUBLESHOOTING FLOWCHART 3

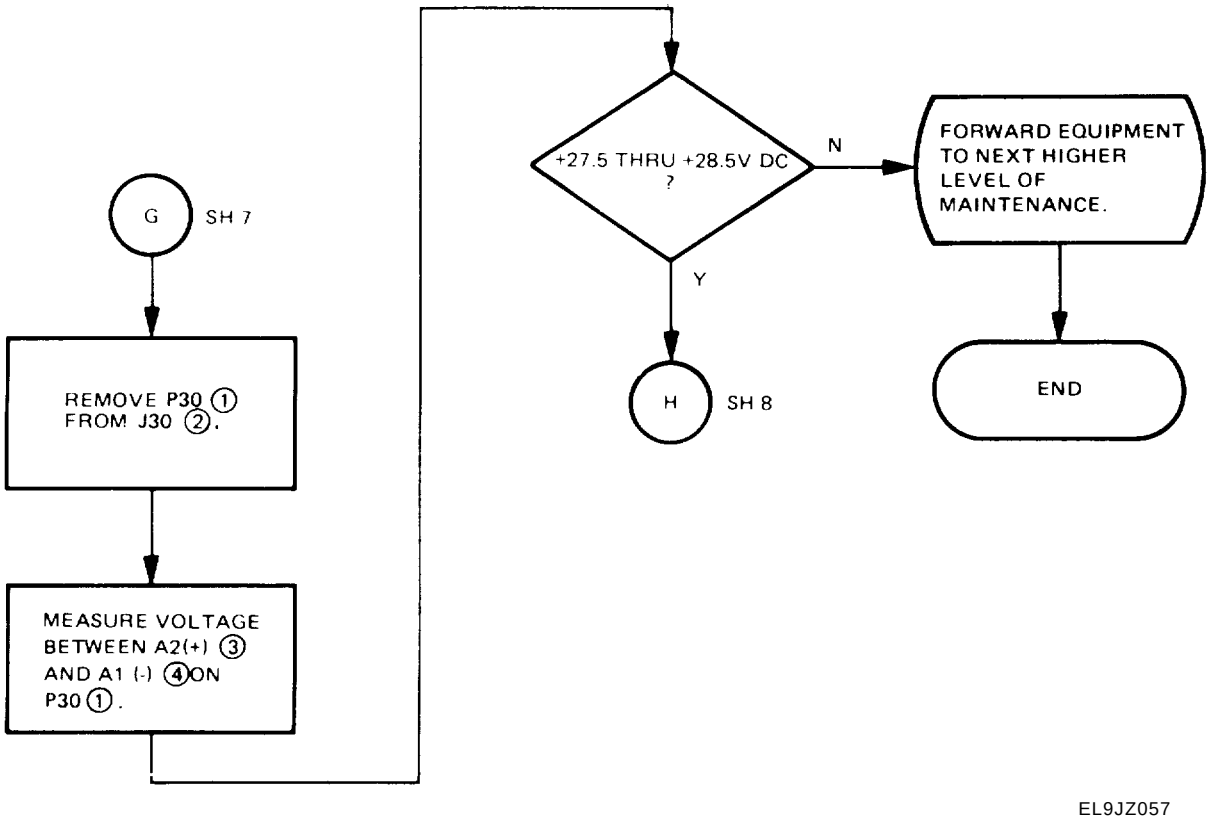
PWR ON/RESET INDICATOR NOT LIT, SEMI MEMORY (SHEET 6 OF 14)



Troubleshooting FLOWCHART 3

PWR ON/RESET INDICATOR NOT LIT, SEMI MEMORY (SHEET 7 OF 14)

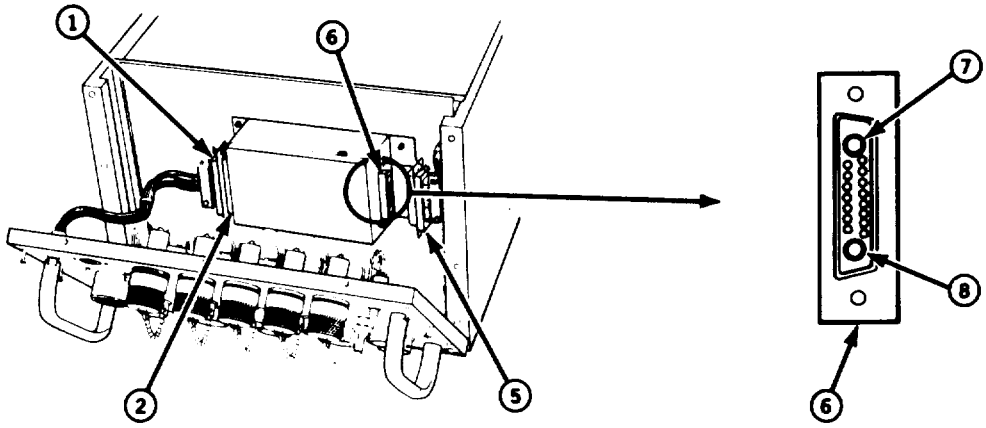


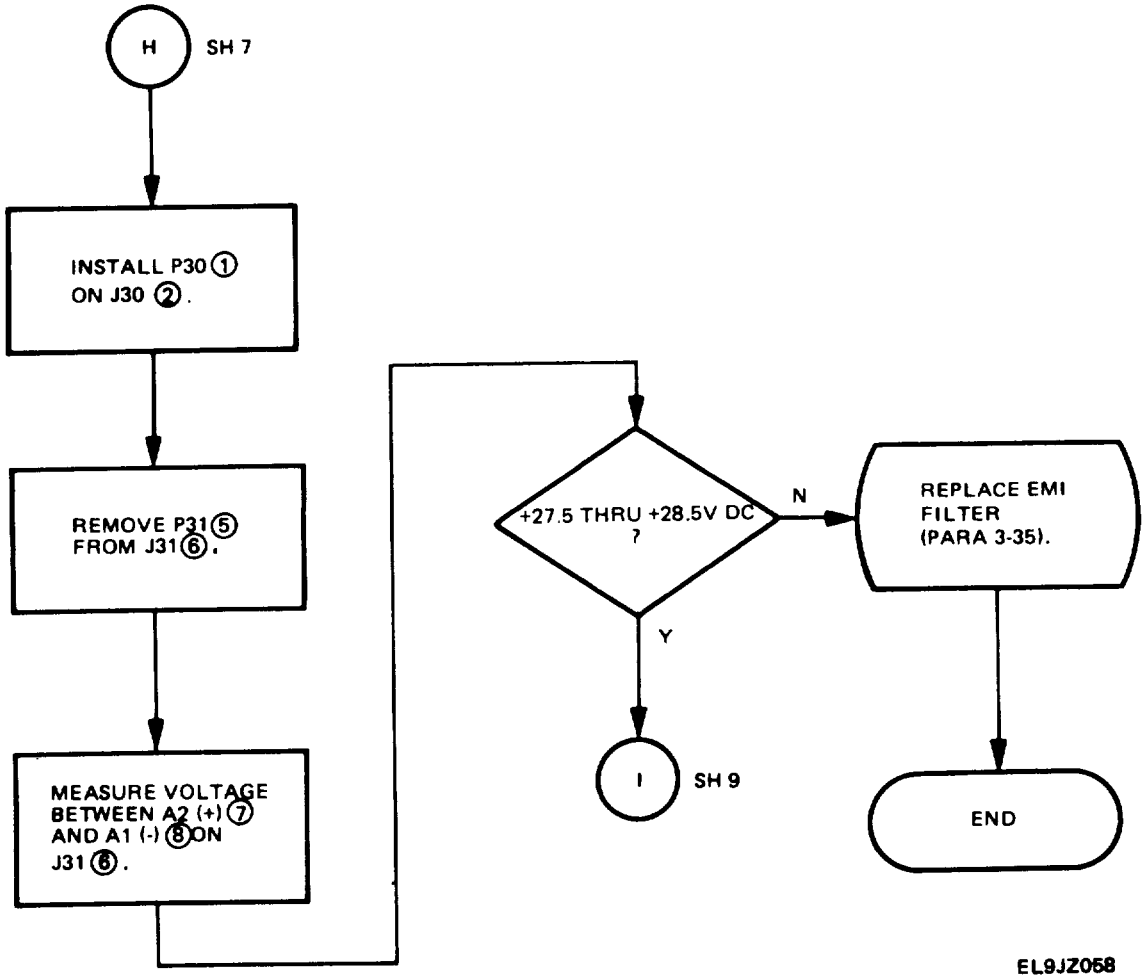


EL9JZ057

TROUBLESHOOTING FLOWCHART 3

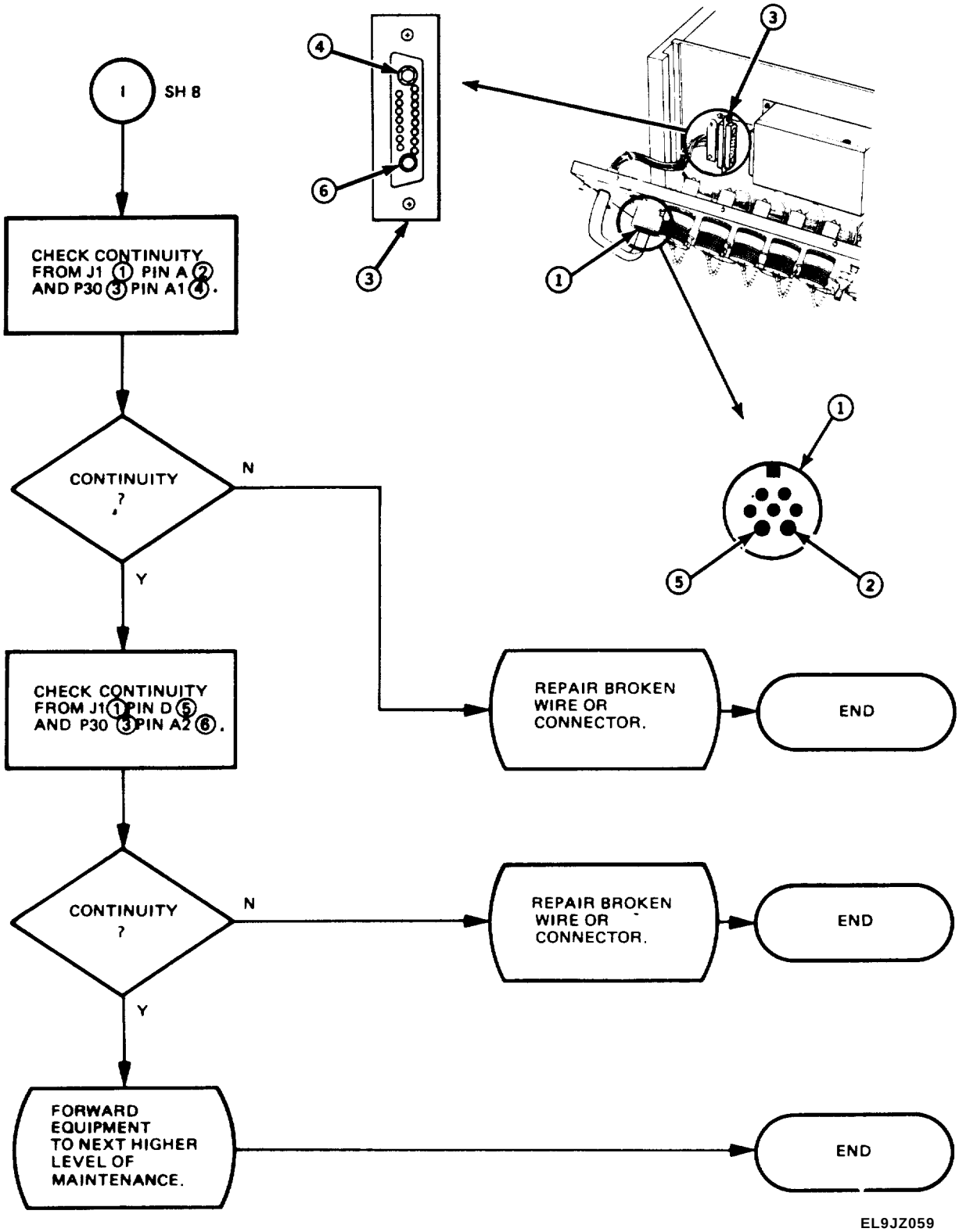
PWR ON/RESET INDICATOR NOT LIT, SEMI MEMORY (SHEET 8 OF 14)





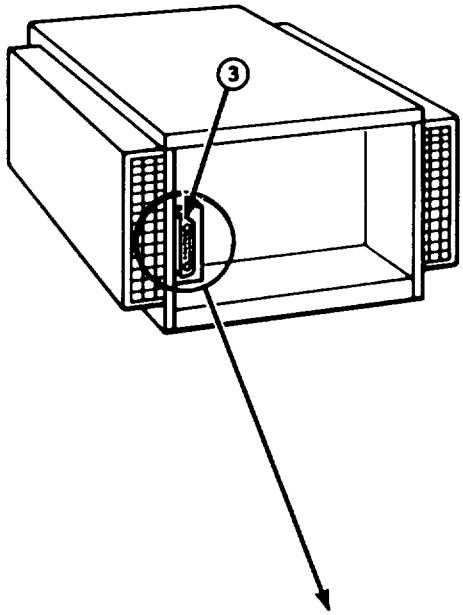
TROUBLESHOOTING FLOWCHART 3

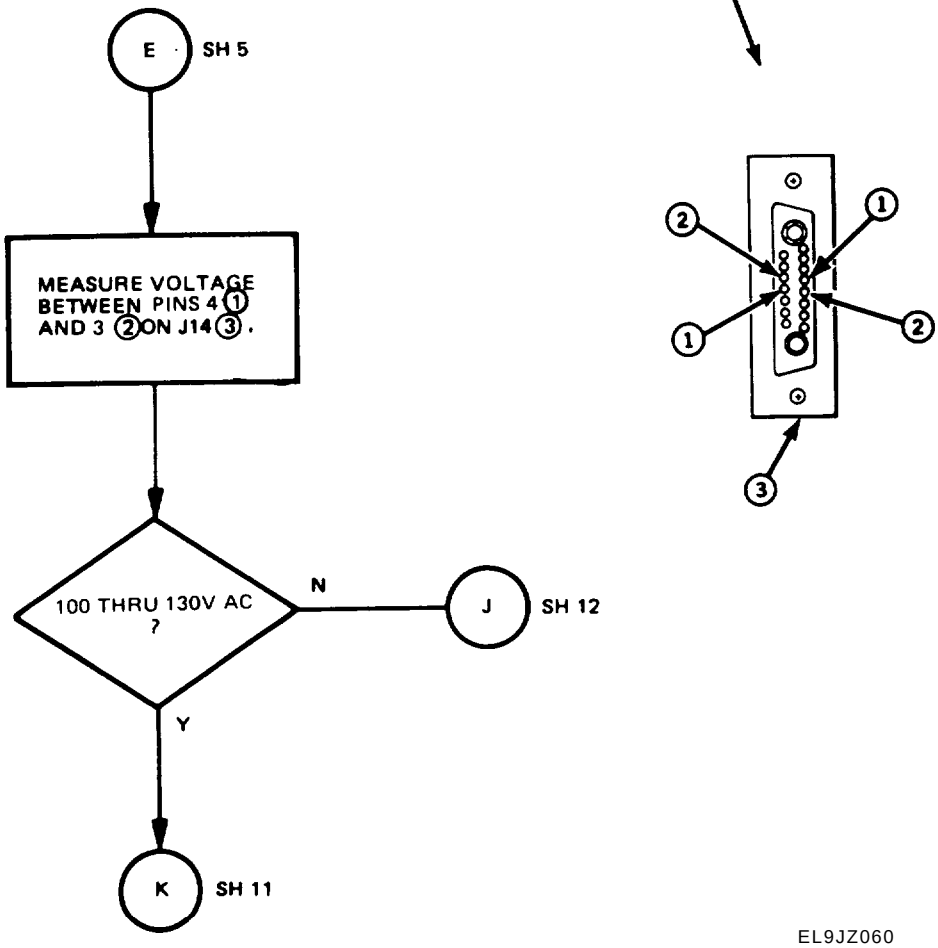
PWR ON/RESET INDICATOR NOT LIT, SEMI MEMORY (SHEET 9 OF 14)



TROUBLESHOOTING FLOWCHART 3

PWR ON/RESET INDICATOR NOT LIT, SEMI MEMORY (SHEET 10 OF 14)

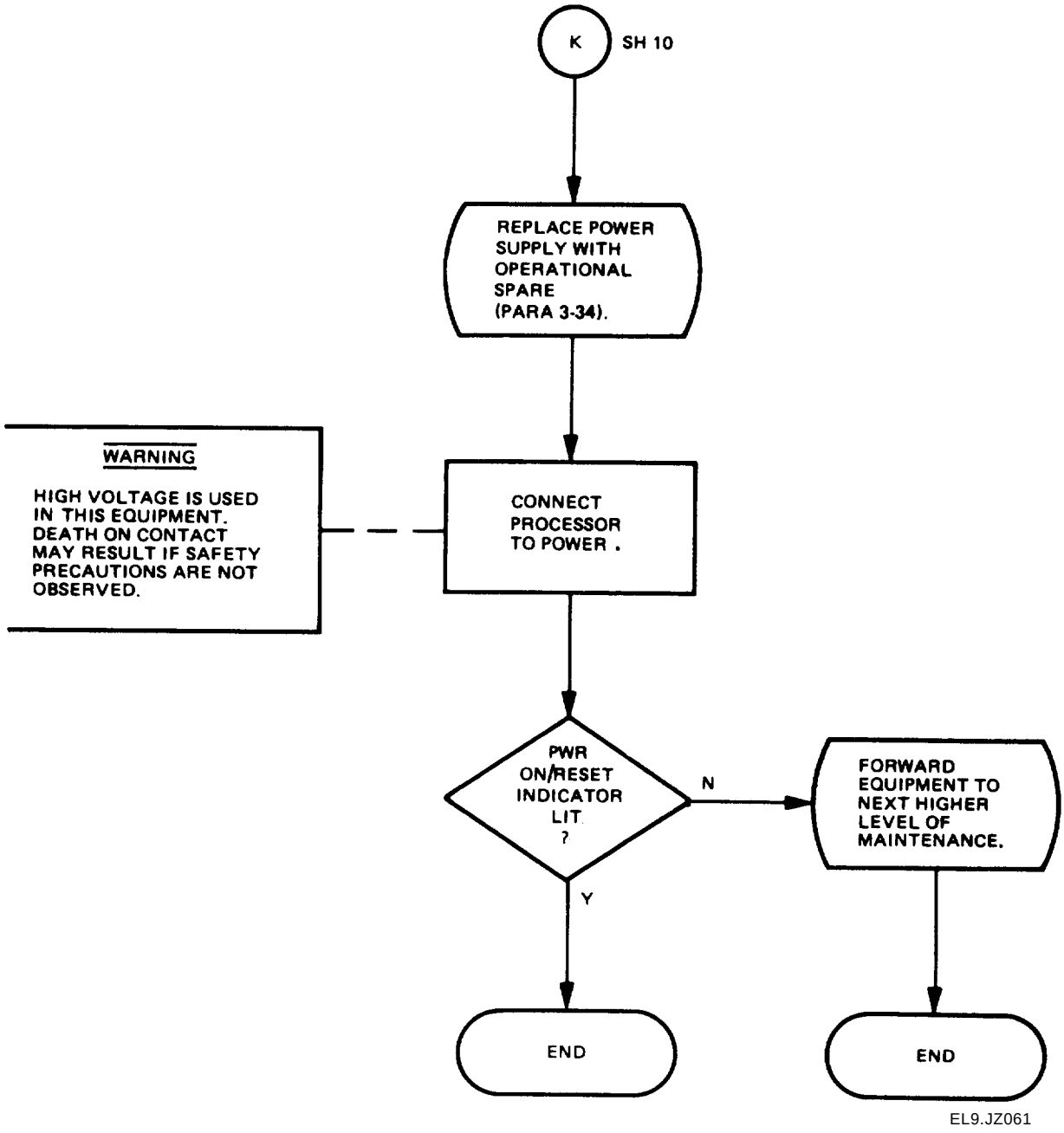




EL9JZ060

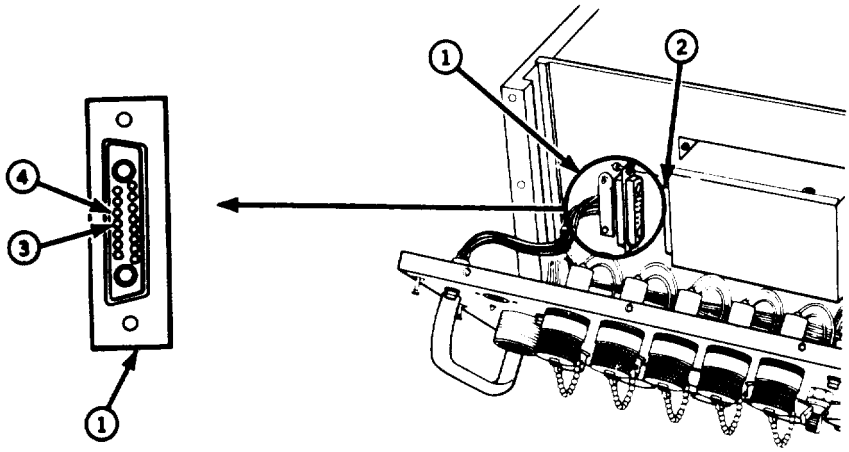
TROUBLESHOOTING FLOWCHART 3

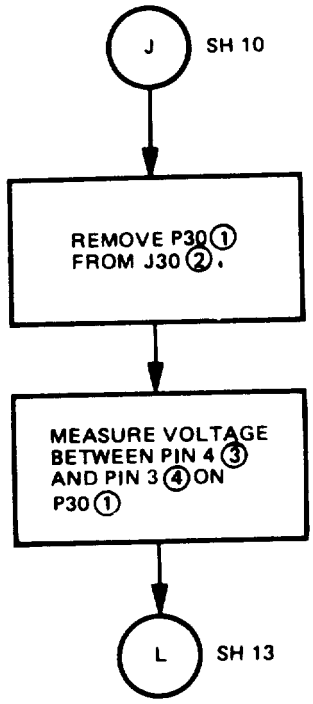
PWR ON/RESET INDICATOR NOT LIT, SEMI MEMORY (SHEET 11 OF 14)



TROUBLESHOOTING FLOWCHART 3

PWR ON/RESET INDICATOR NOT LIT, SEMI MEMORY (SHEET 12 OF 14)

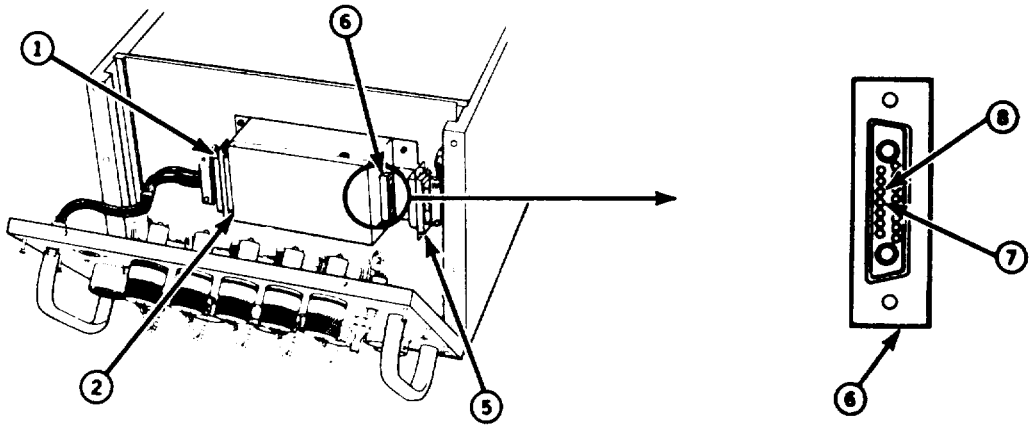


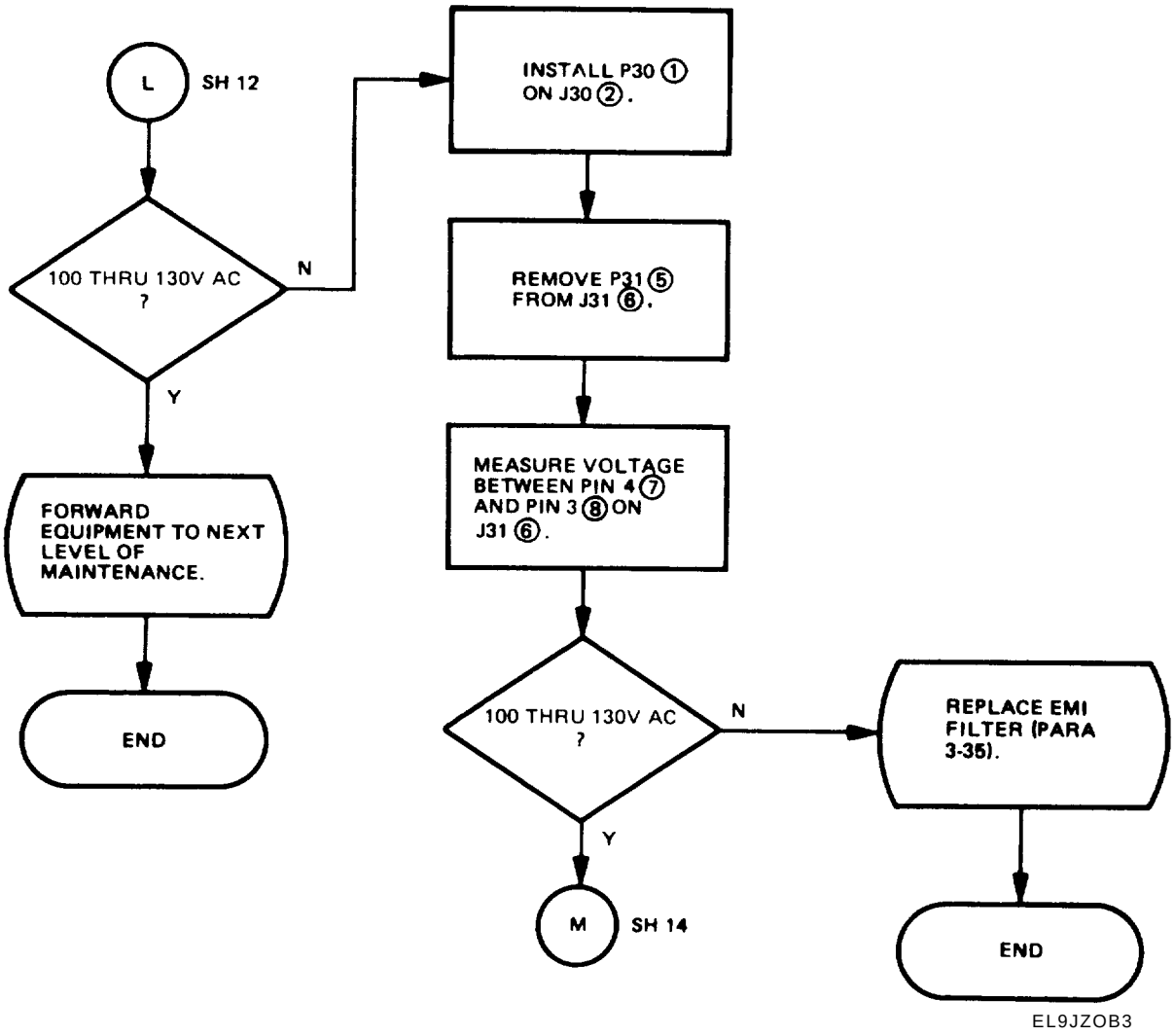


EL9JZ062

TROUBLESHOOTING FLOWCHART 3

PWR ON/RESET INDICATOR NOT LIT, SEMI MEMORY (SHEET 13 OF 14)

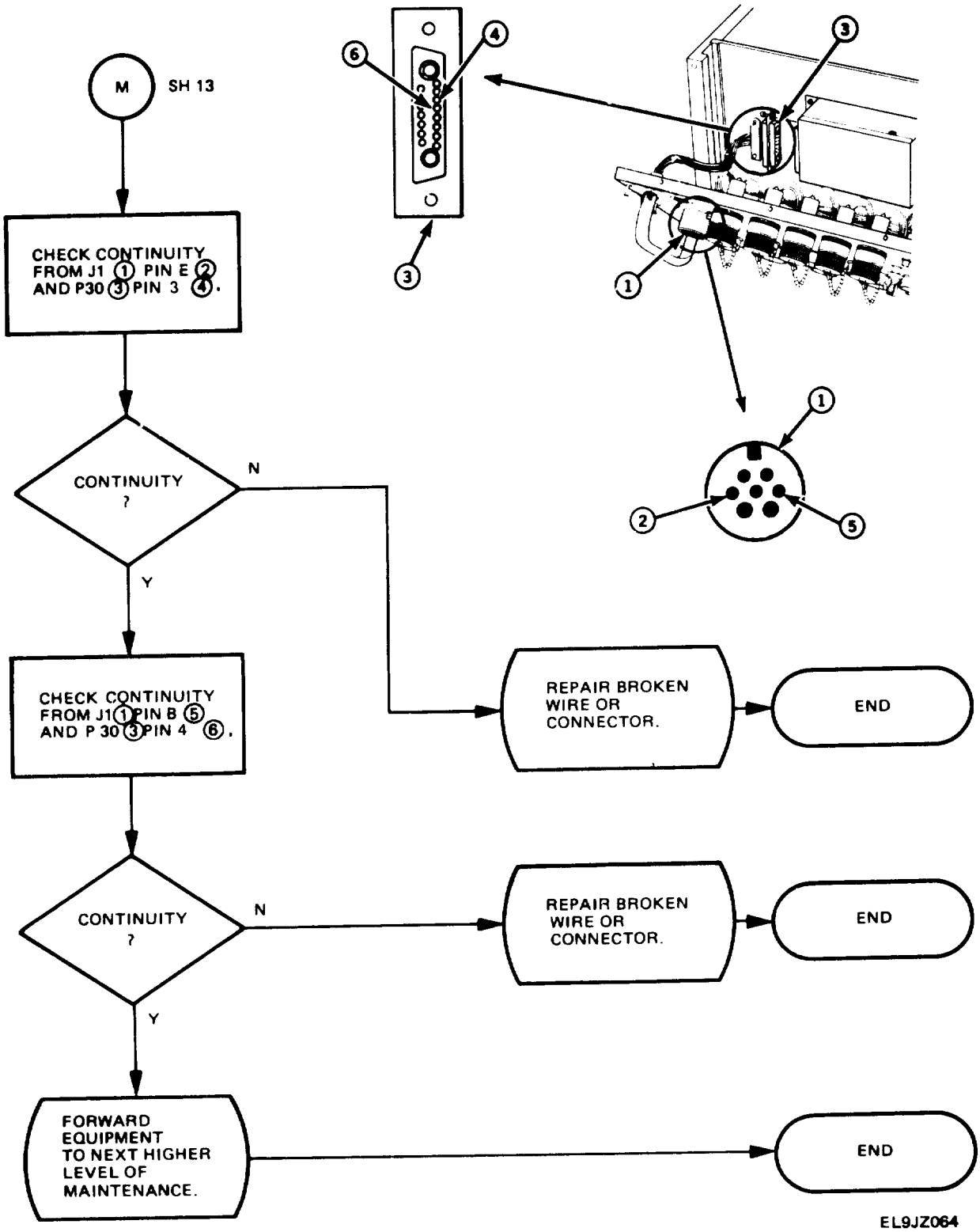




EL9JZOB3

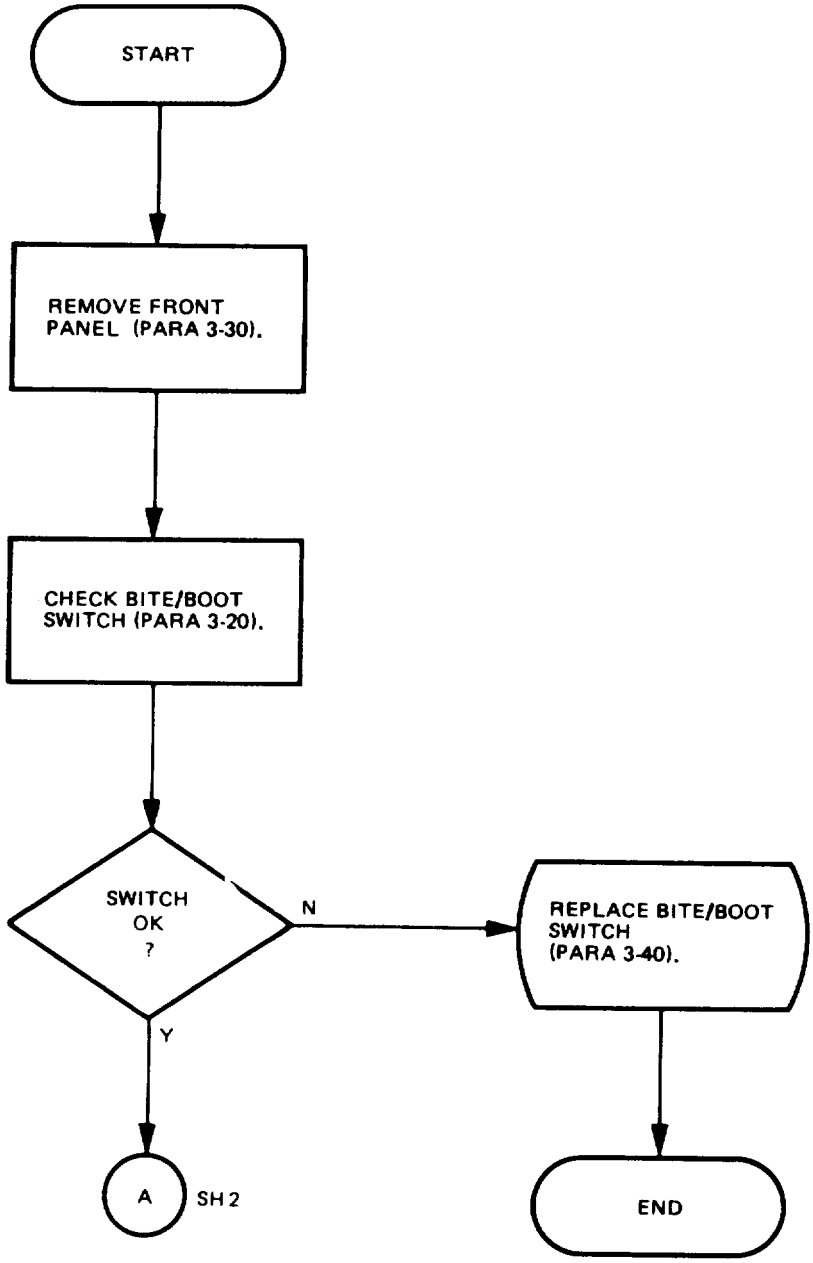
TROUBLESHOOTING FLOWCHART 3

PWR ON/RESET INDICATOR NOT LIT, SEMI MEMORY (SHEET 14 OF 14)



TROUBLESHOOTING FLOWCHART 4

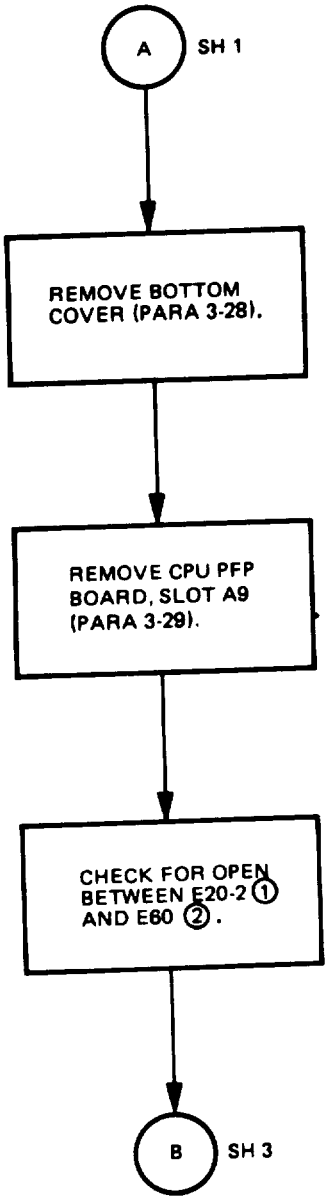
BITE/BOOT INDICATOR NOT LIT, CORE MEMORY (SHEET 1 OF 4)

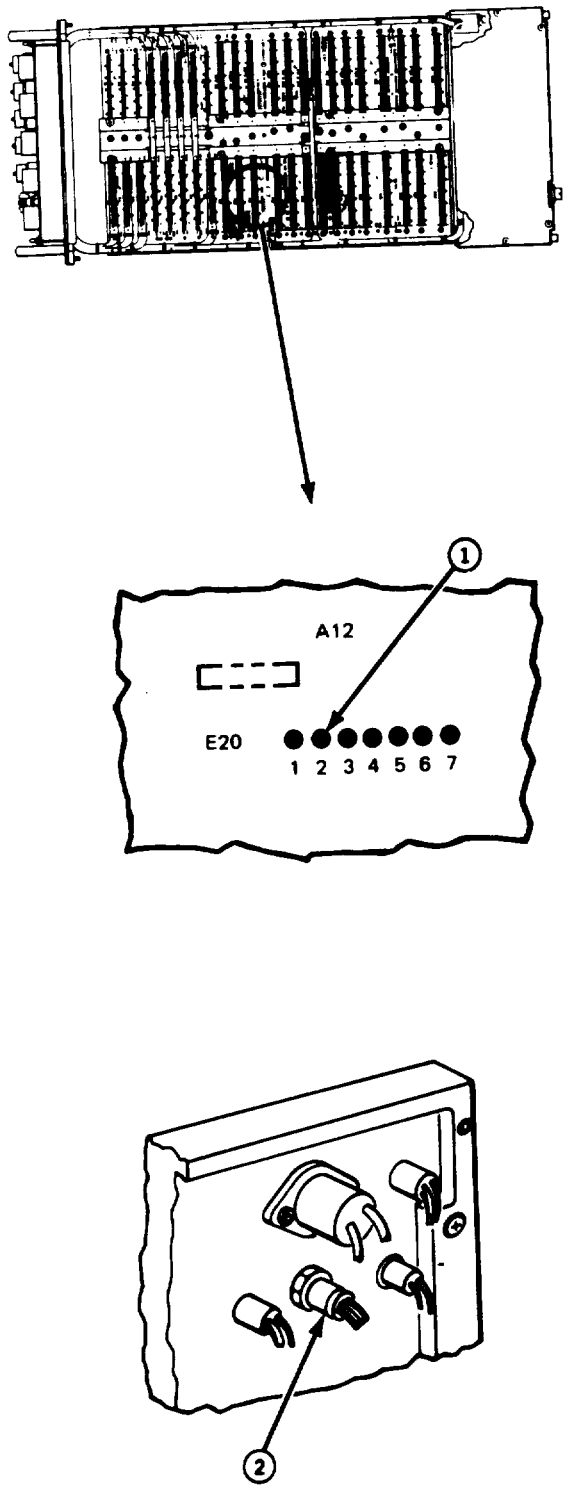


EL9JZ085

TROUBLESHOOTING FLOWCHART 4

BITE/BOOT INDICATOR NOT LIT, CORE MEMORY (SHEET 2 OF 4)

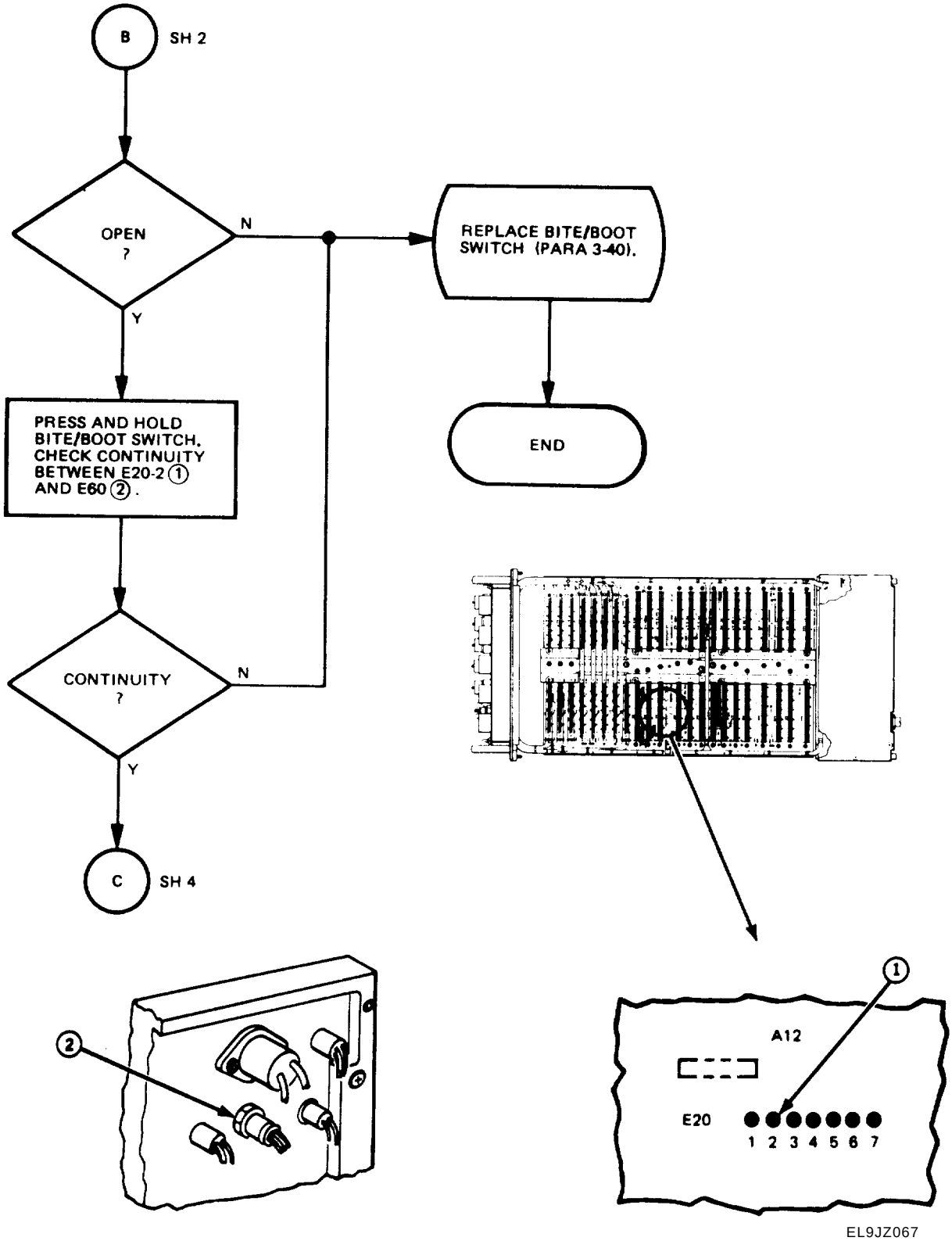




EL9JZ066

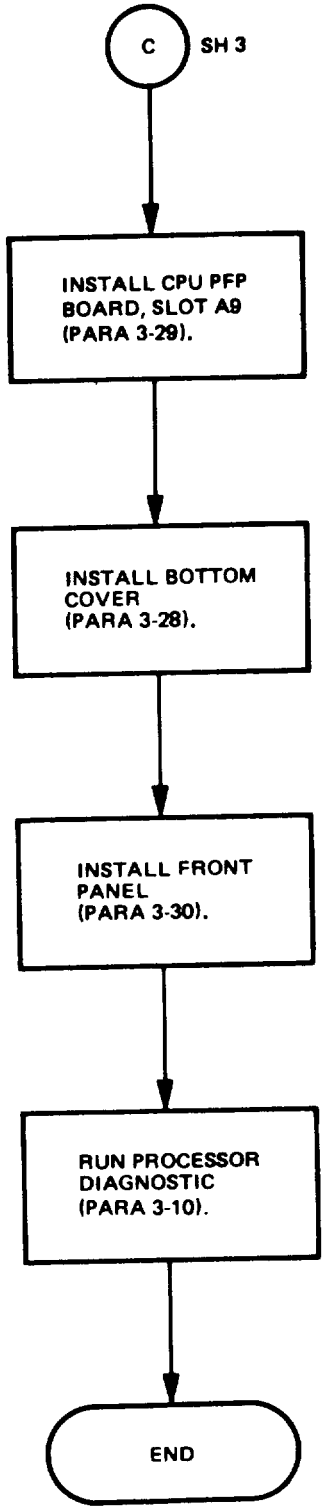
TROUBLESHOOTING FLOWCHART 4

BITE/BOOT INDICATOR NOT LIT, CORE MEMORY (SHEET 3 OF 4)



TROUBLESHOOTING FLOWCHART 4

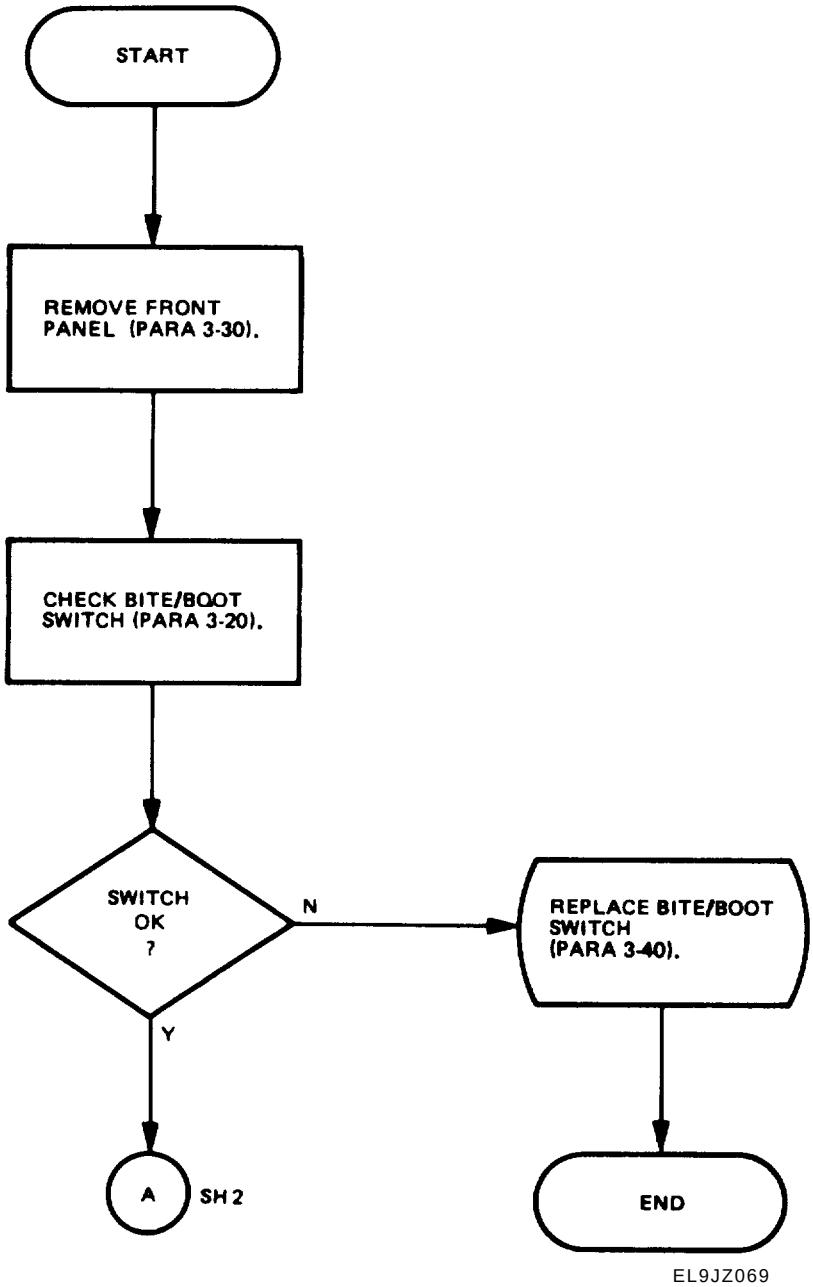
BITE/BOOT INDICATOR NOT LIT, CORE MEMORY (SHEET 4 OF 4)



EL9JZ068

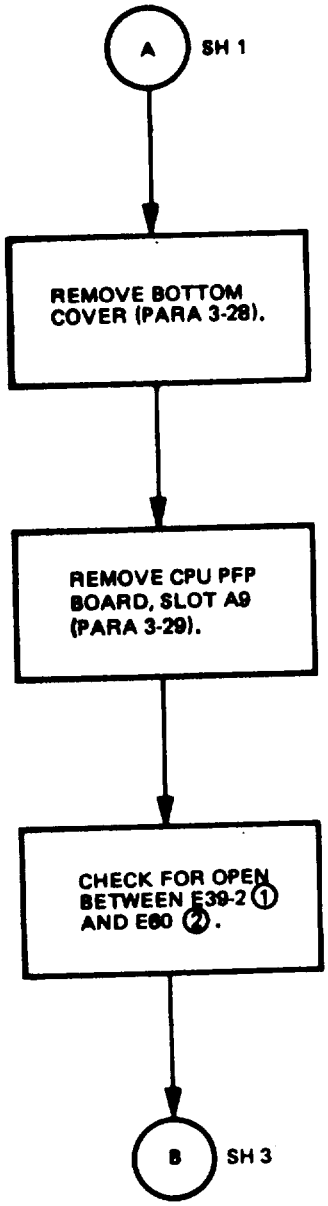
TROUBLESHOOTING FLOWCHART 5

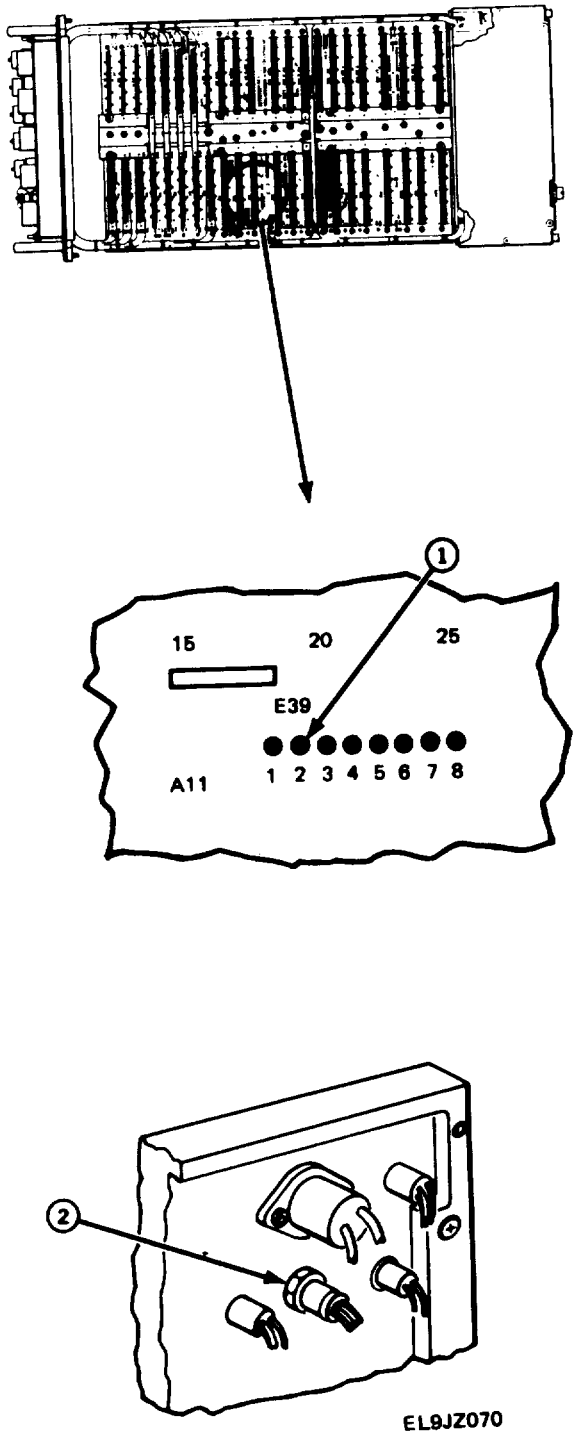
BITE/BOOT INDICATOR NOT LIT, SEMI MEMORY (SHEET 1 OF 4)



TROUBLESHOOTING FLOWCHART 5

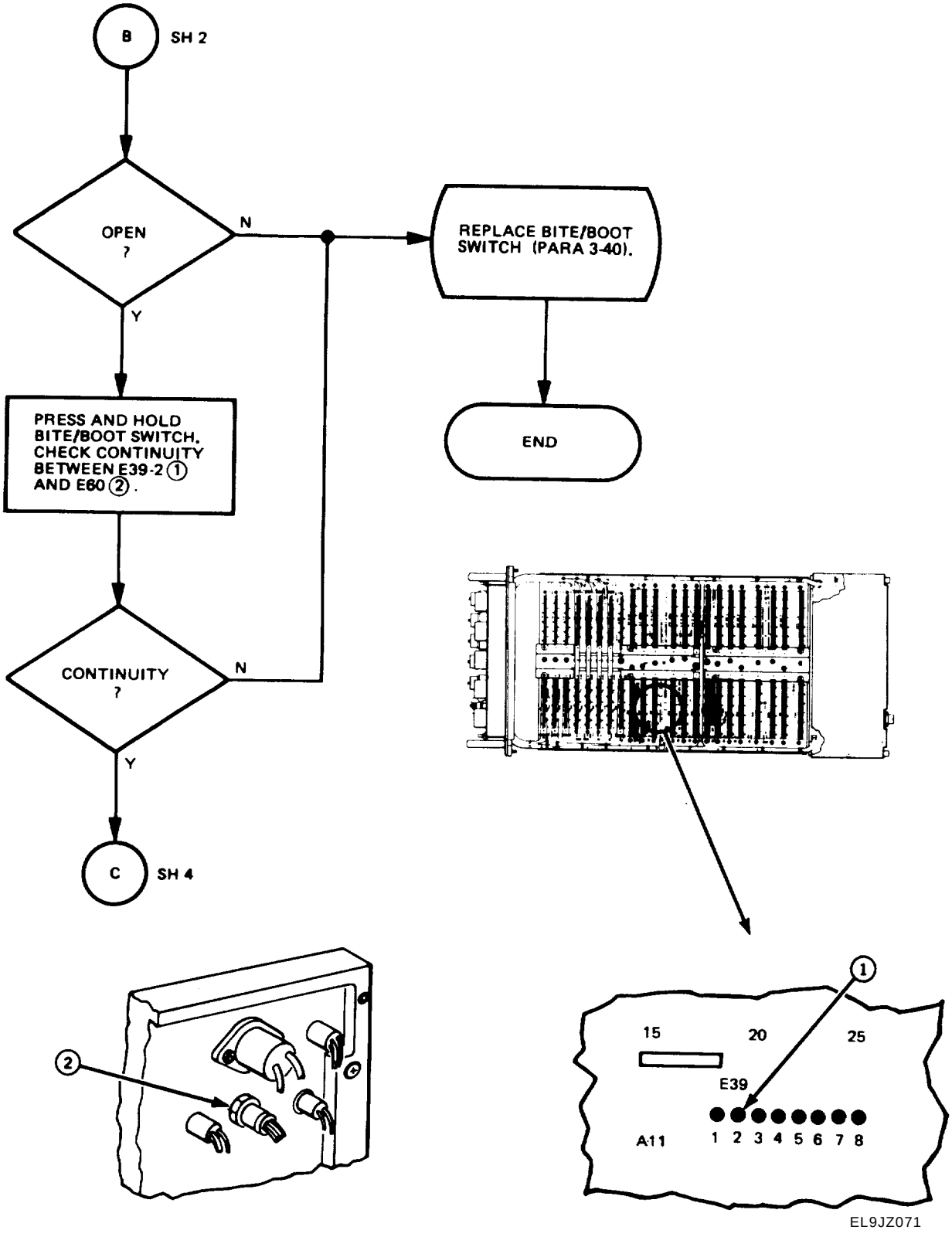
BITE/BOOT INDICATOR NOT LIT, SEMI MEMORY (SHEET 2 OF 4)





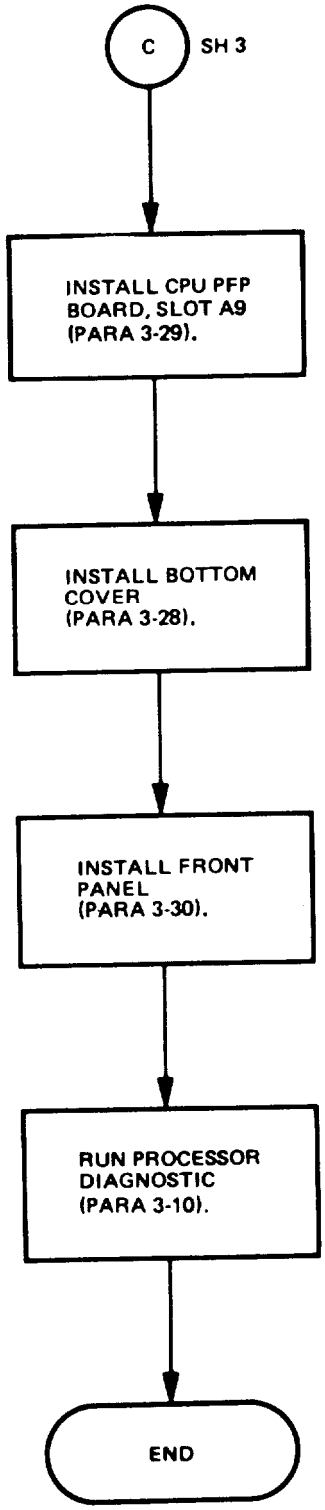
TROUBLESHOOTING FLOWCHART 5

BITE/BOOT INDICATOR NOT LIT, SEMI MEMORY (SHEET 3 OF 4)



TROUBLESHOOTING FLOWCHART 5

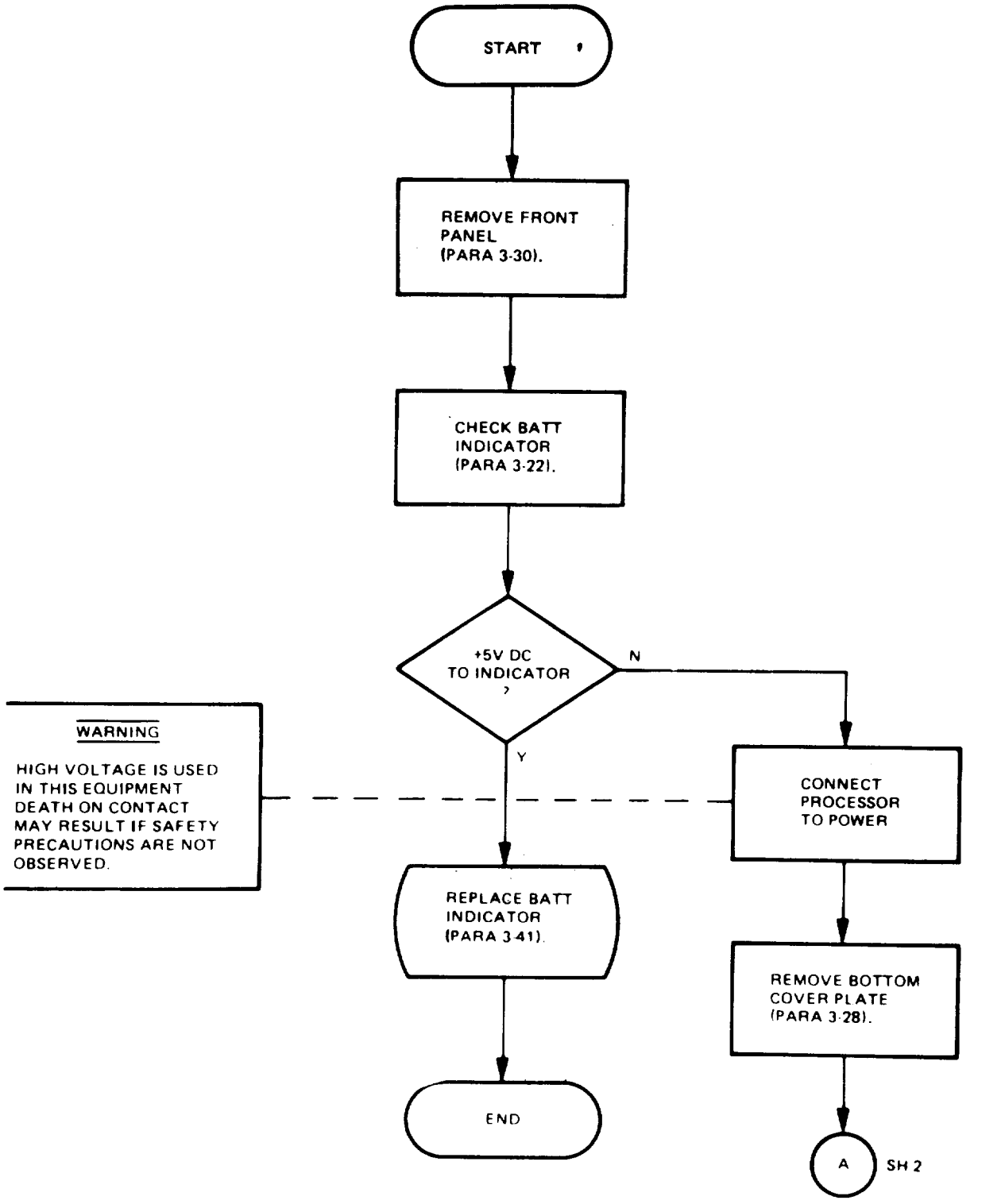
BITE/BOOT INDICATOR NOT LIT, SEMI MEMORY (SHEET 4 OF 4)



EL9JZ072

TROUBLESHOOTING FLOWCHART 6

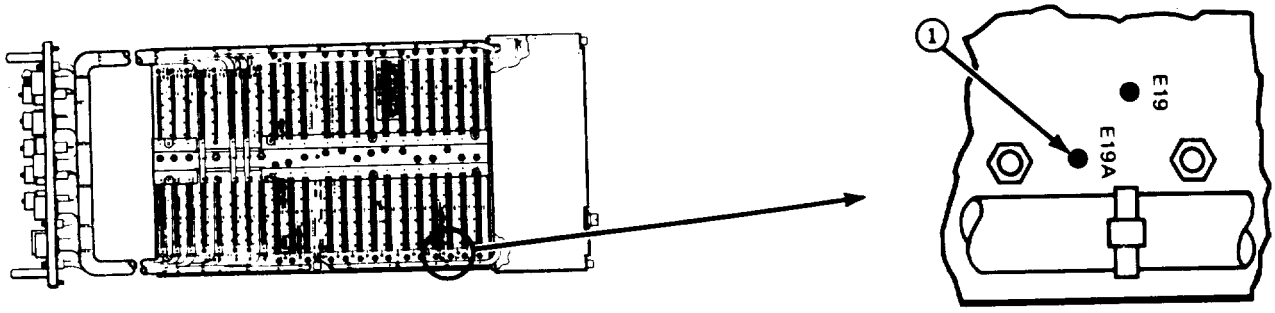
BATT INDICATOR NOT LIT, SEMI MEMORY (SHEET 1 OF 13)

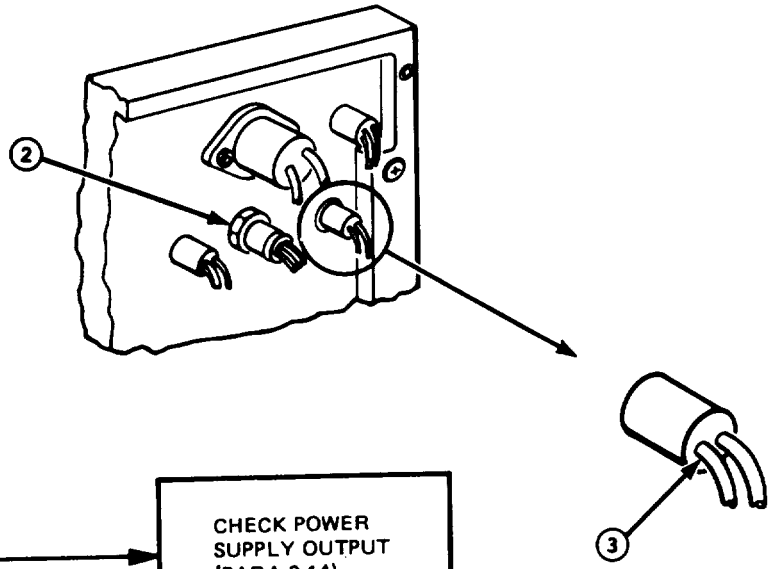


E L9JZ073

TROUBLESHOOTING FLOWCHART 6

BATT INDICATOR NOT LIT, SEMI MEMORY (SHEET 2 OF 13)

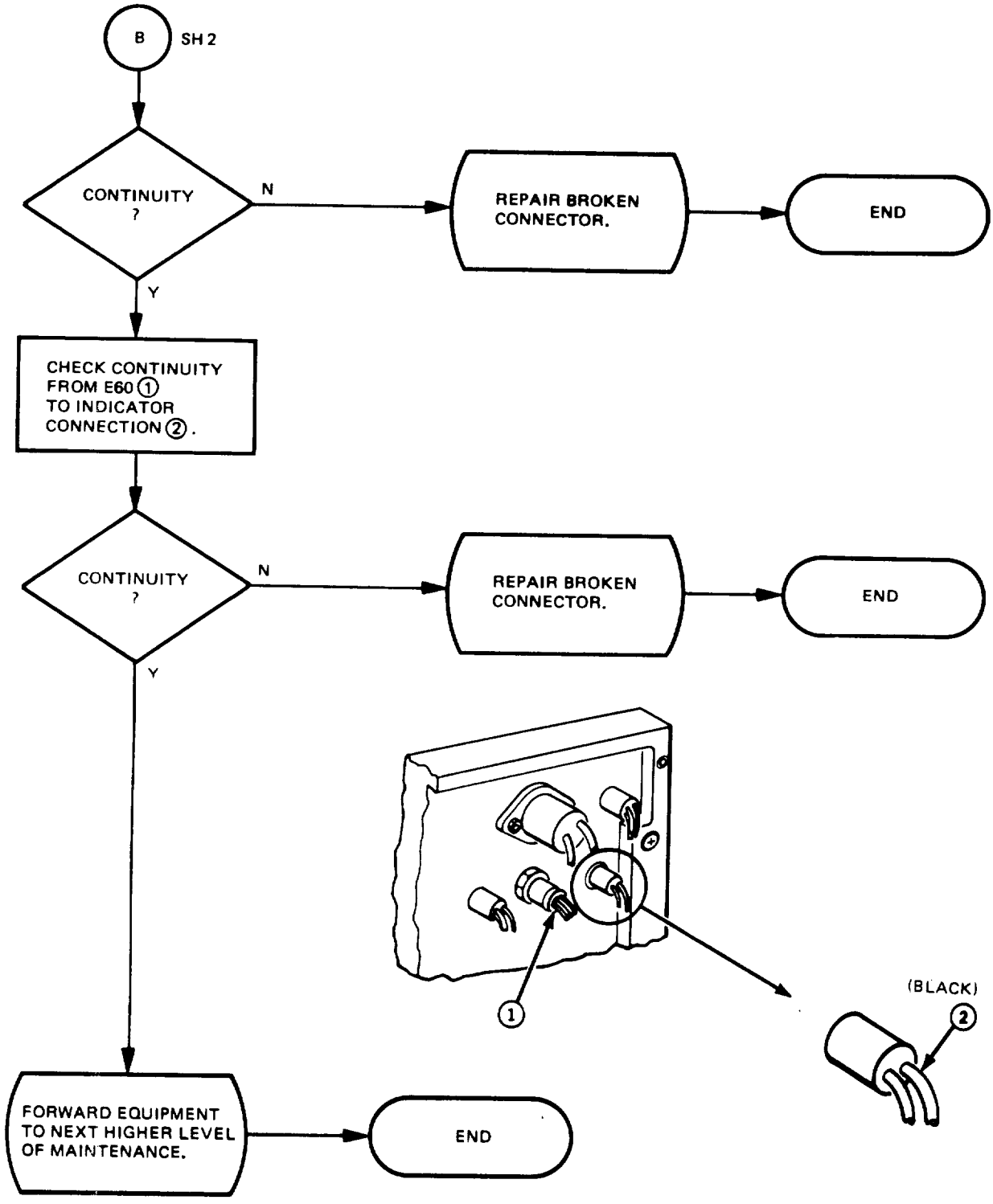




EL9JZ074

TROUBLESHOOTING FLOWCHART 6

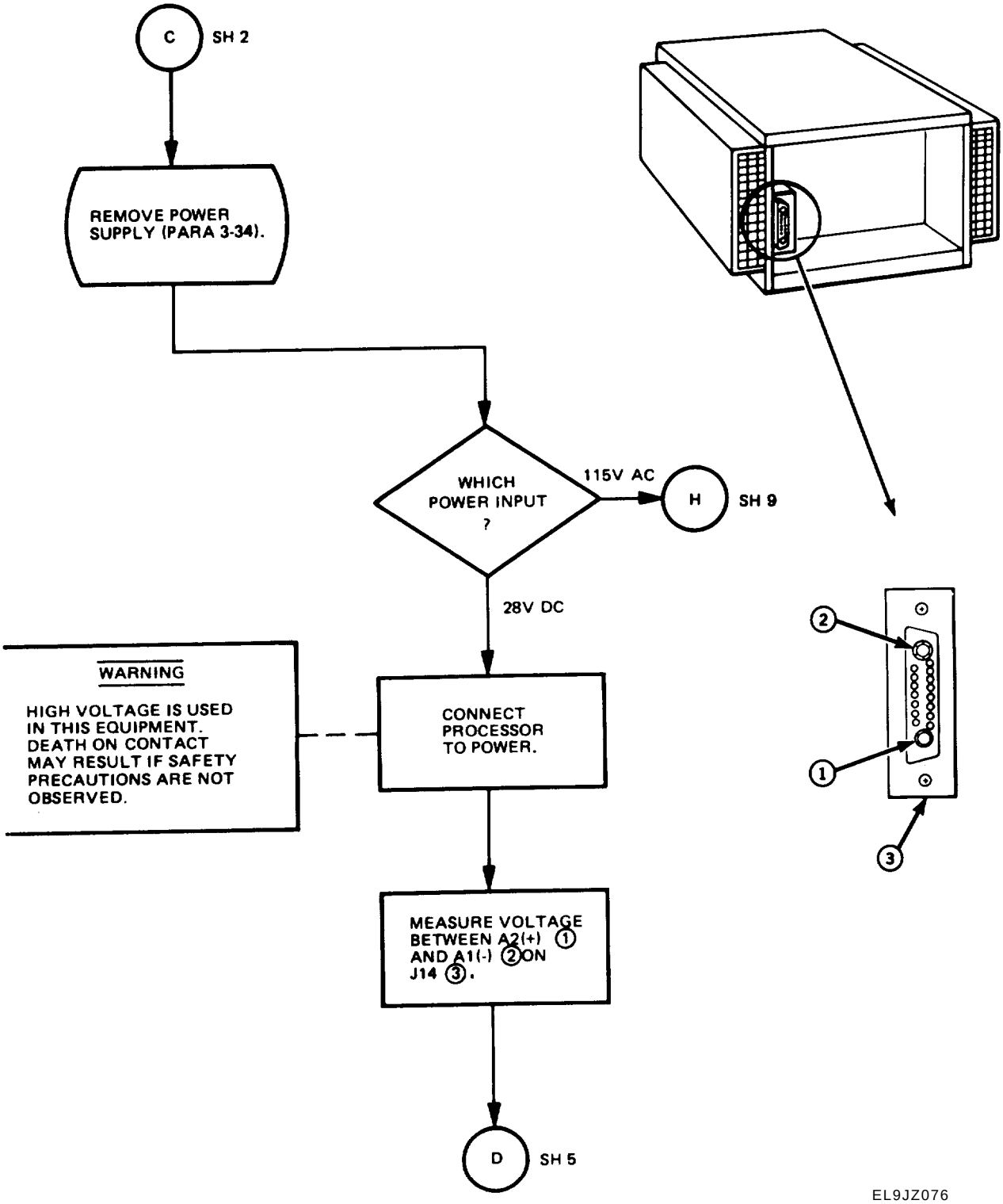
BATT INDICATOR NOT LIT, SEMI MEMORY (SHEET 3 OF 13)



EL9JZ075

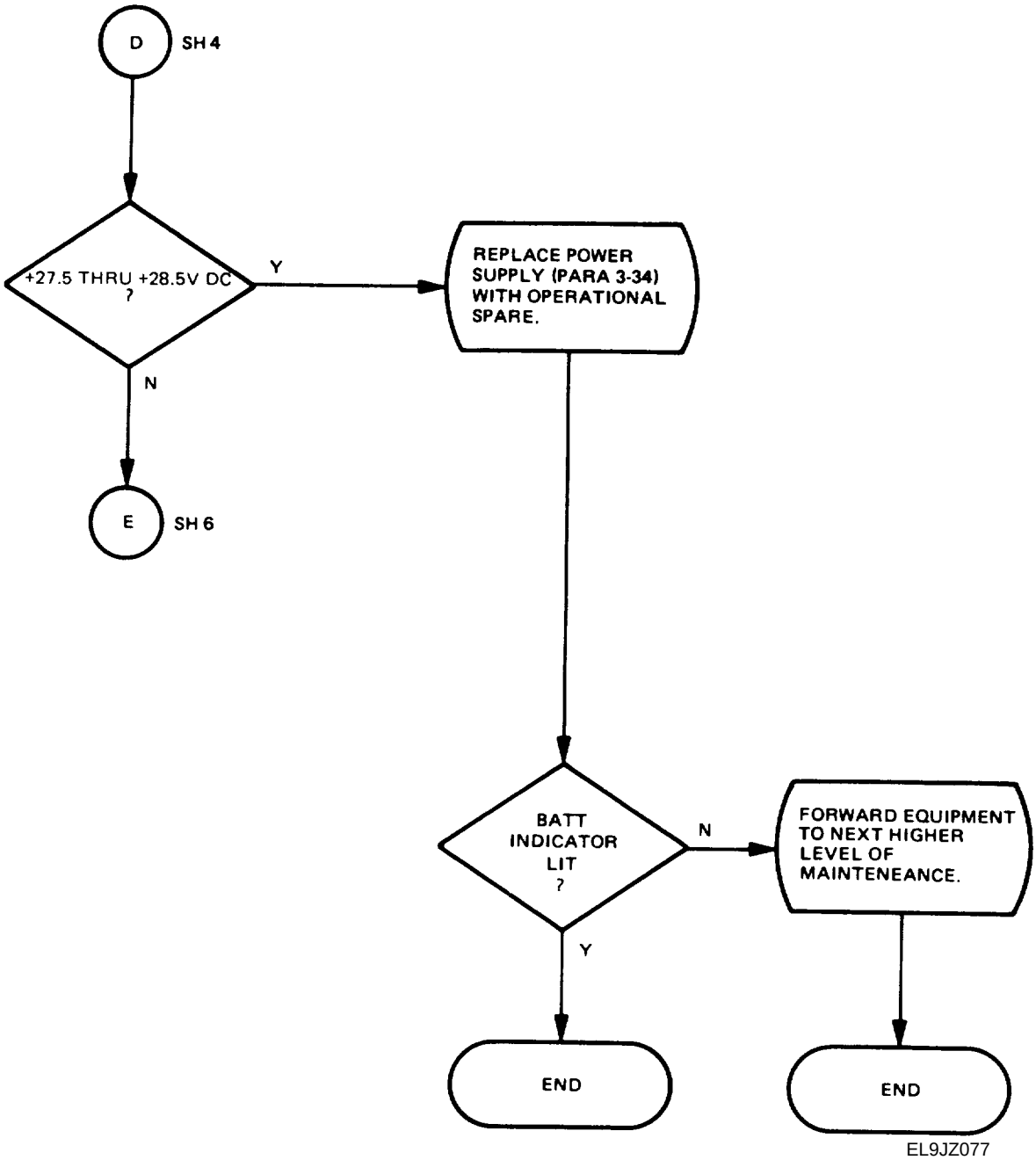
TROUBLESHOOTING FLOWCHART 6

BATT INDICATOR NOT LIT, SEMI MEMORY (SHEET 4 OF 13)



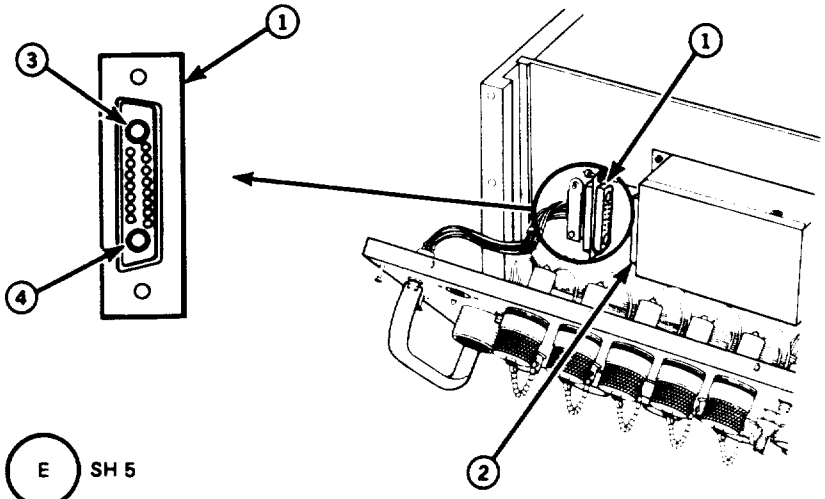
TROUBLESHOOTING FLOWCHART 6

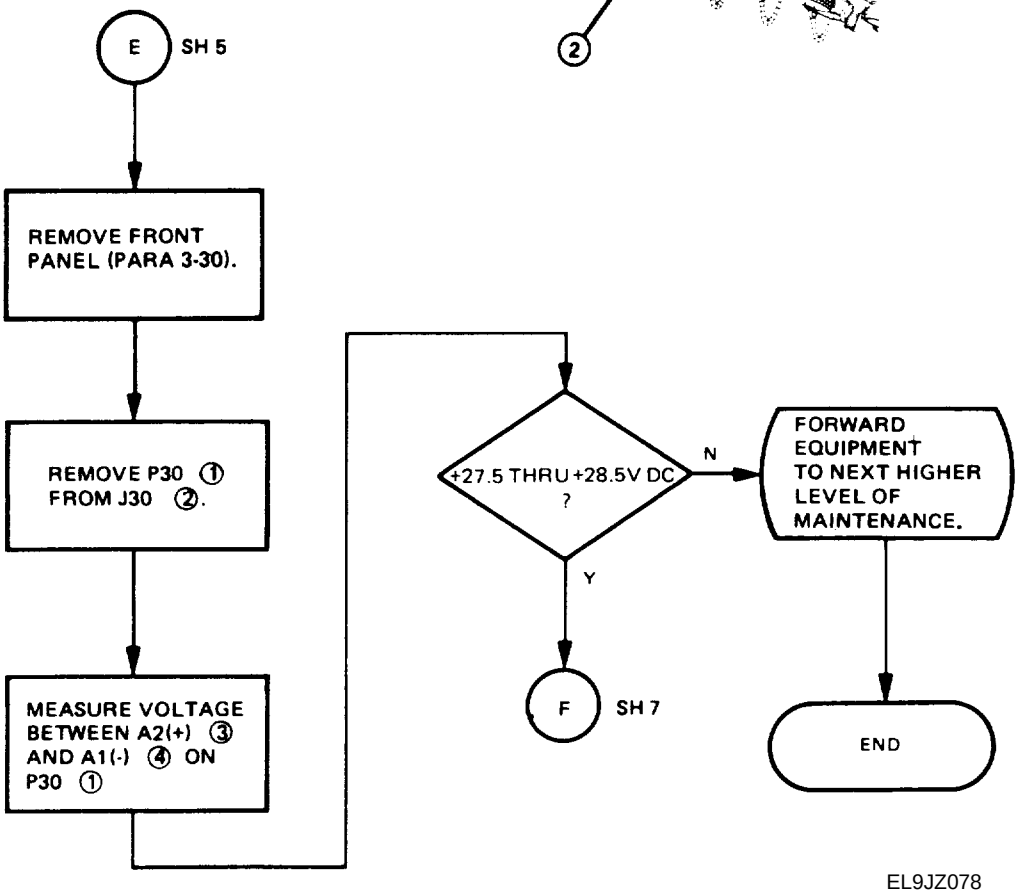
BATT INDICATOR NOT LIT, SEMI MEMORY (SHEET 5 OF 13)



TROUBLESHOOTING FLOWCHART 6

BATT INDICATOR NOT LIT, SEMI MEMORY (SHEET 6 OF 13)

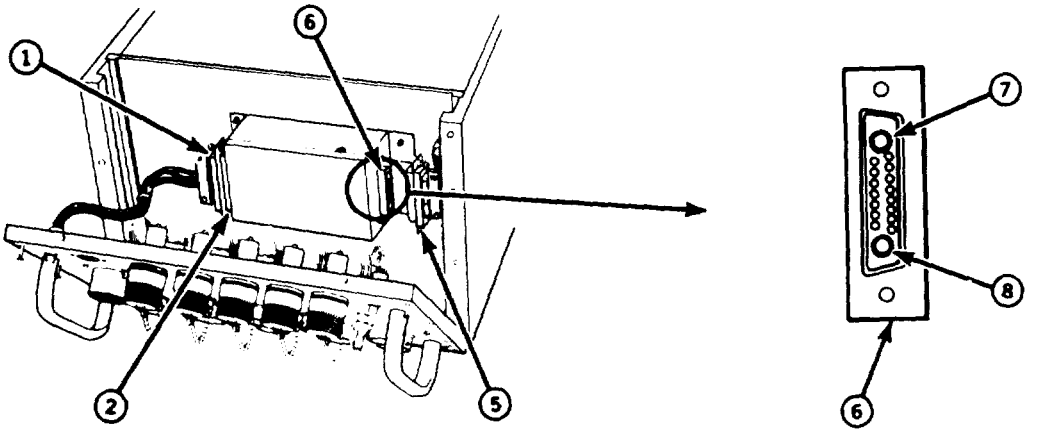


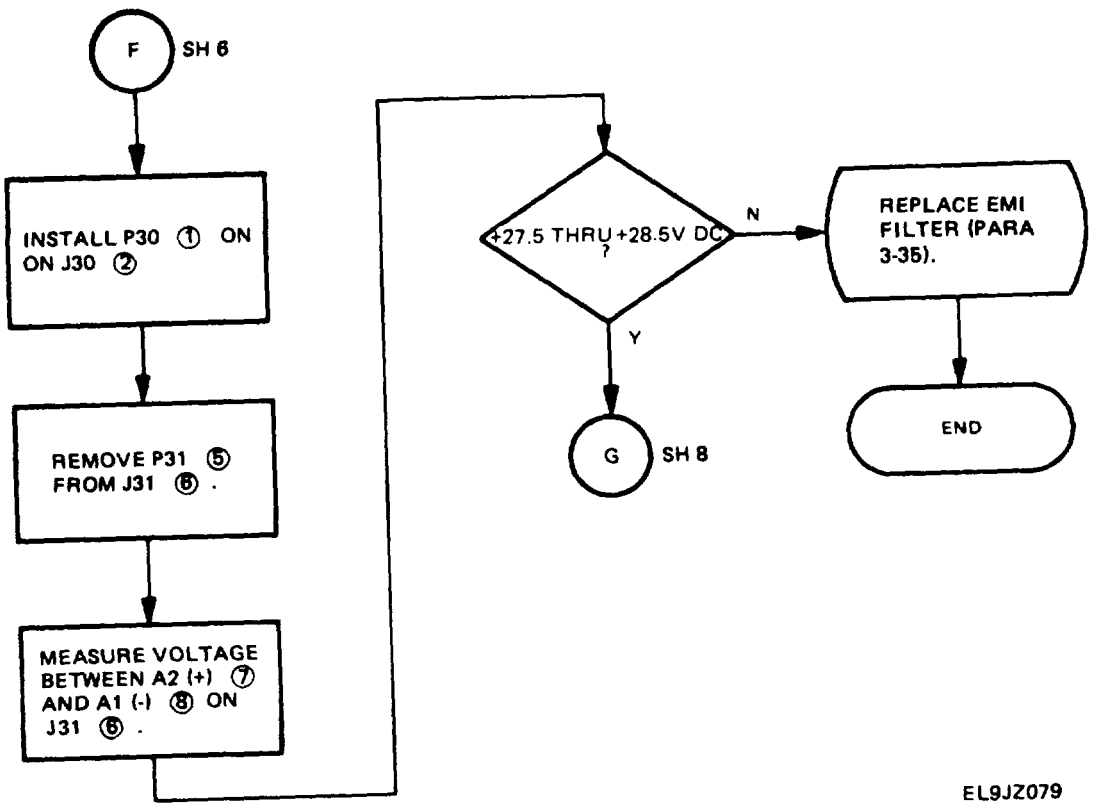


EL9JZ078

TROUBLESHOOTING FLOWCHART 6

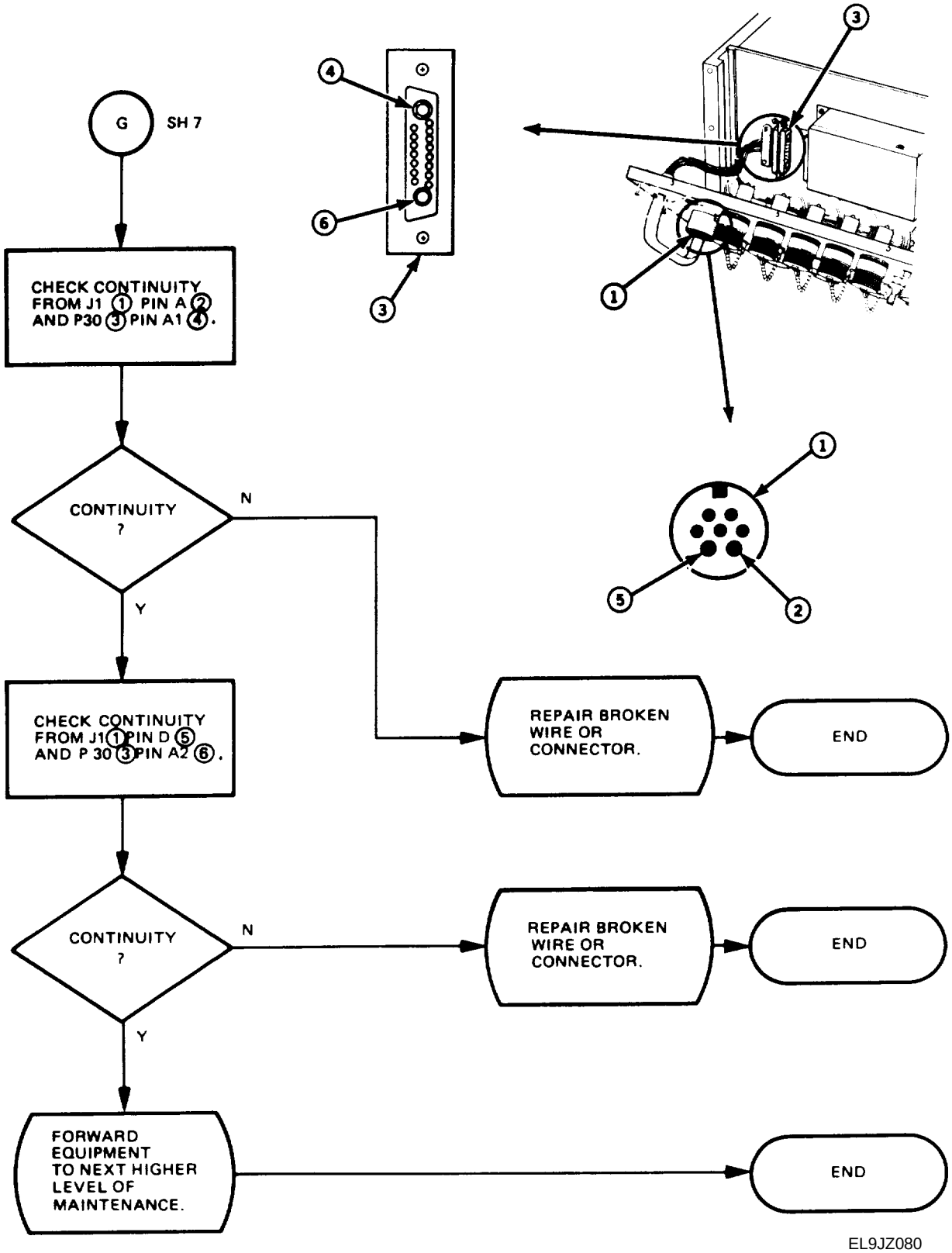
BATT INDICATOR NOT LIT, SEMI MEMORY (SHEET 7 OF 13)





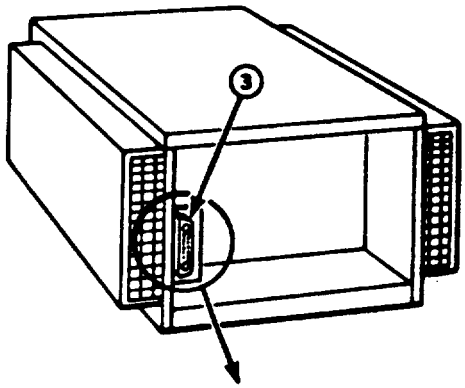
TROUBLESHOOTING FLOWCHART 6

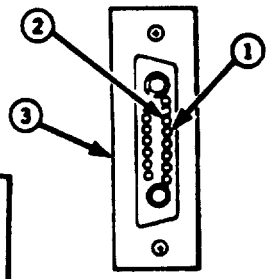
BATT INDICATOR NOT LIT, SEMI MEMORY (SHEET 8 OF 13)



TROUBLESHOOTING FLOWCHART 6

BATT INDICATOR NOT LIT, SEMI MEMORY (SHEET 9 OF 13)





H SH 4

WARNING

HIGH VOLTAGE IS USED IN THIS EQUIPMENT DEATH ON CONTACT MAY RESULT IF SAFETY PRECAUTIONS ARE NOT OBSERVED.

CONNECT PROCESSOR TO POWER

MEASURE VOLTAGE BETWEEN POINTS 4 (1) AND 3 (2) ON J14 (3).

100 THRU 130V AC ?

N

J SH 11

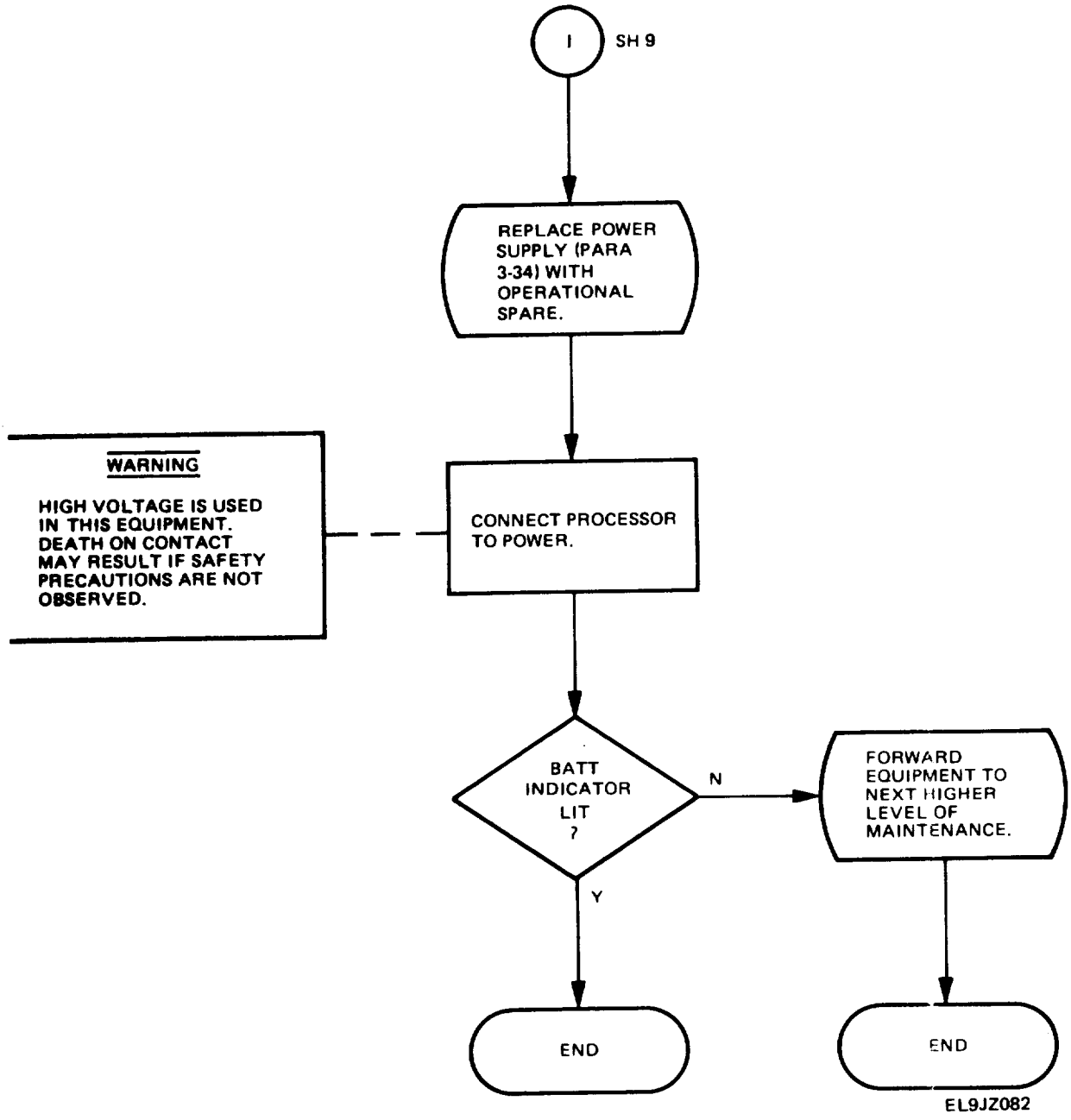
Y

I SH 10

EL9JZ081

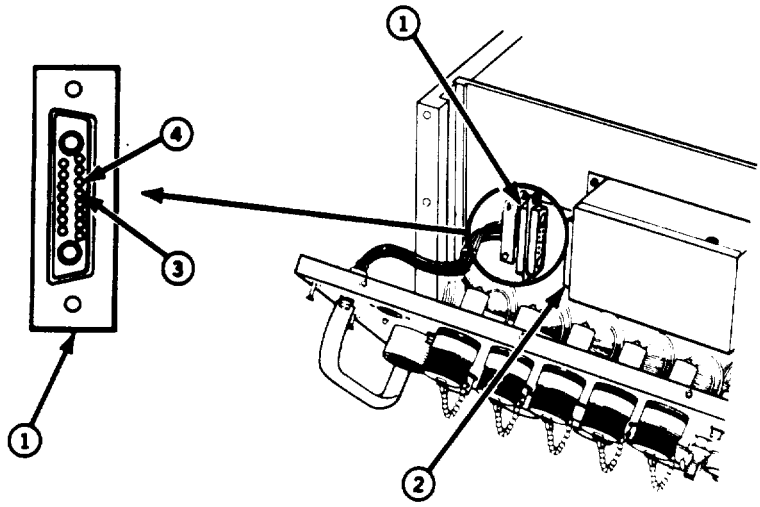
TROUBLESHOOTING FLOWCHART 6

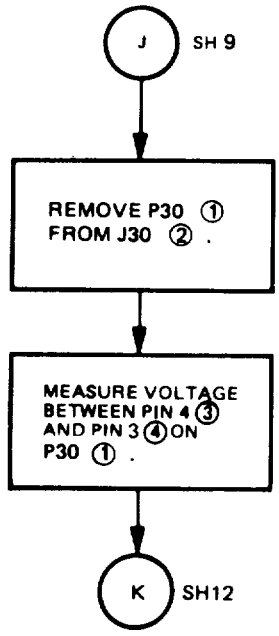
BAIT INDICATOR NOT LIT, SEMI MEMORY (SHEET 10 OF 13)



TROUBLESHOOTING FLOWCHART 6

BATT INDICATOR NOT LIT, SEMI MEMORY (SHEET 11 OF 13)

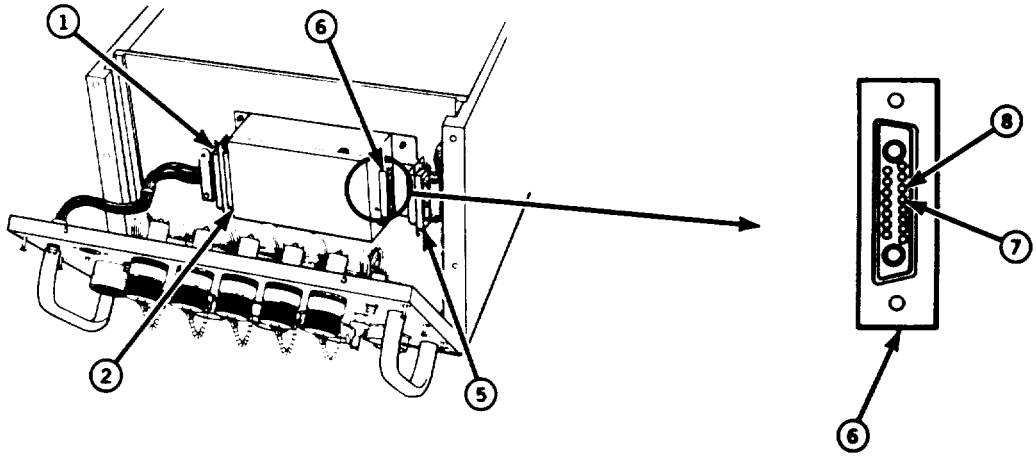


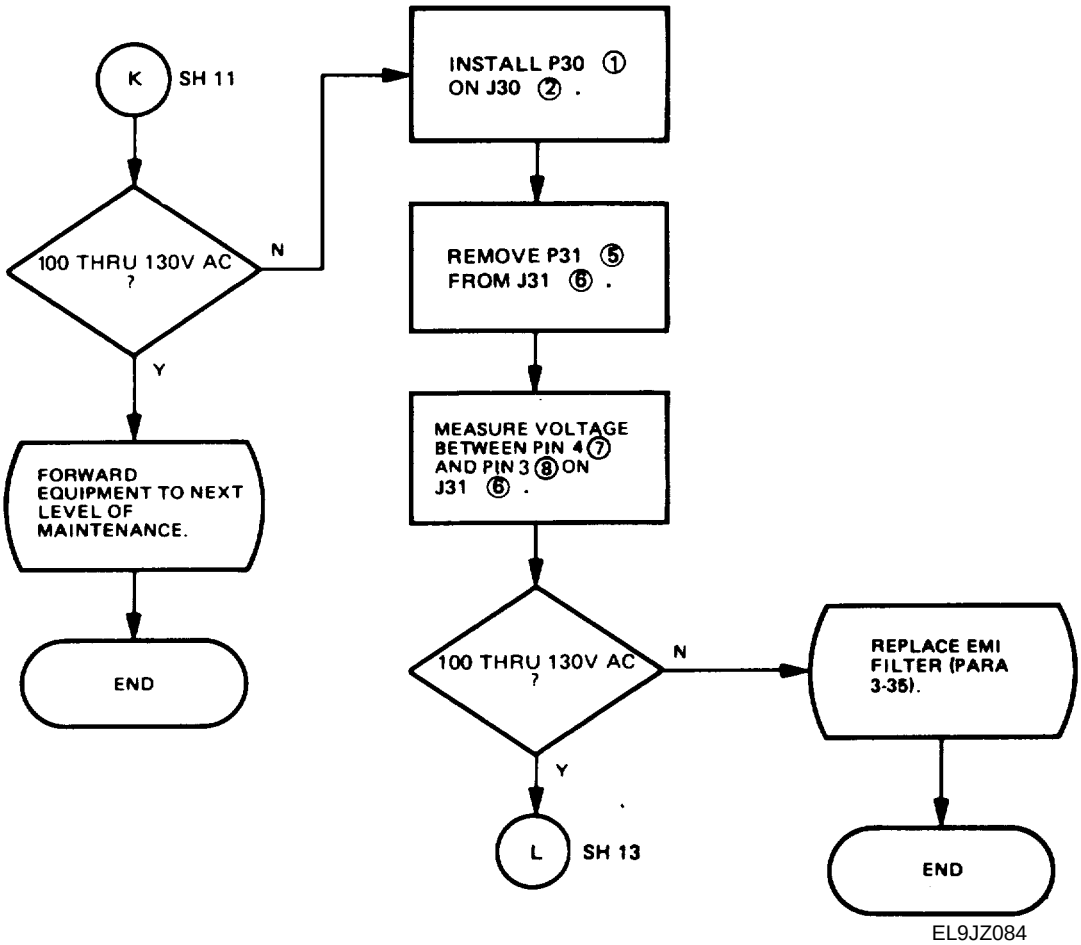


EL9JZ083

TROUBLESHOOTING FLOWCHART 6

BATT INDICATOR NOT LIT, SEMI MEMORY (SHEET 12 OF 13)

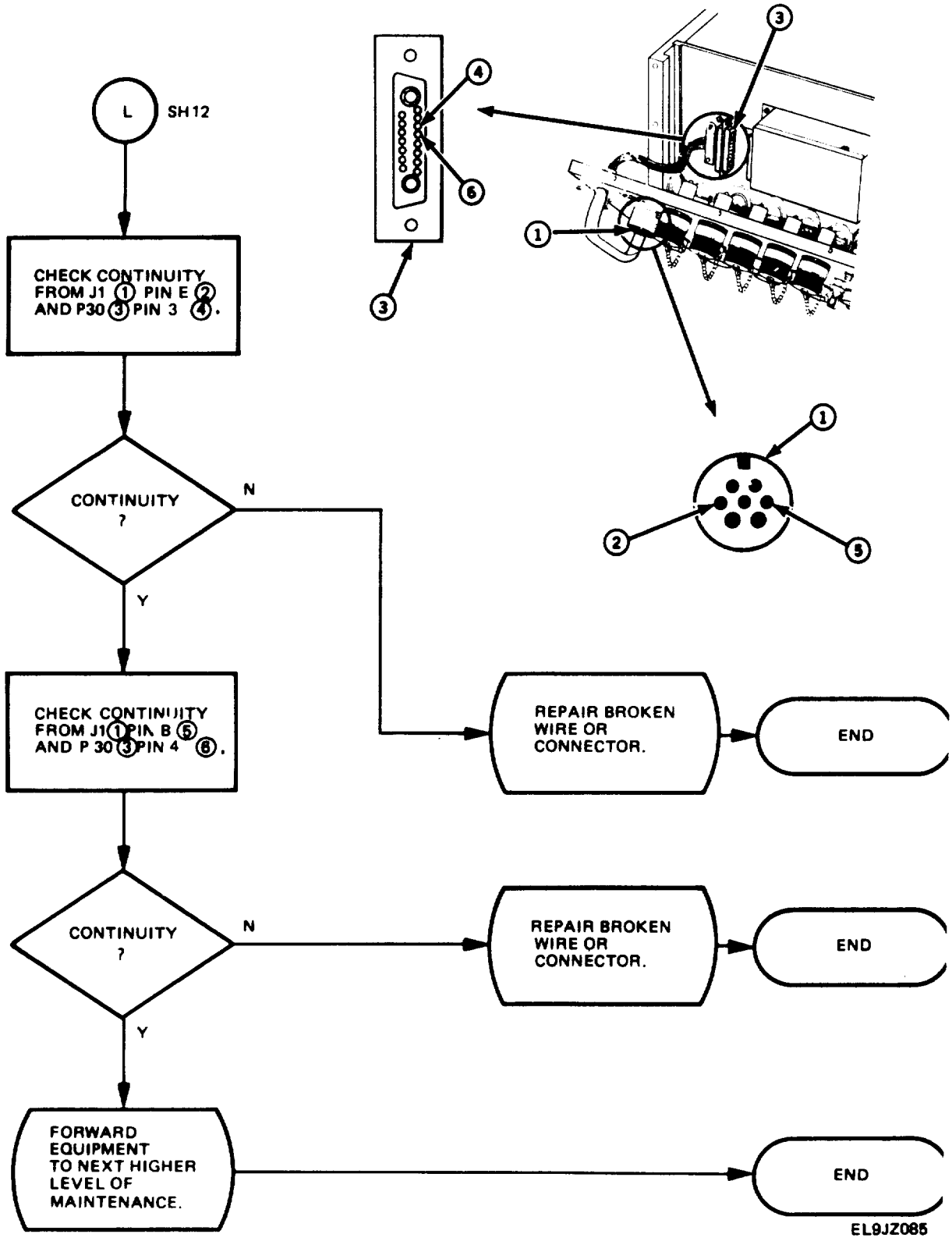




EL9JZ084

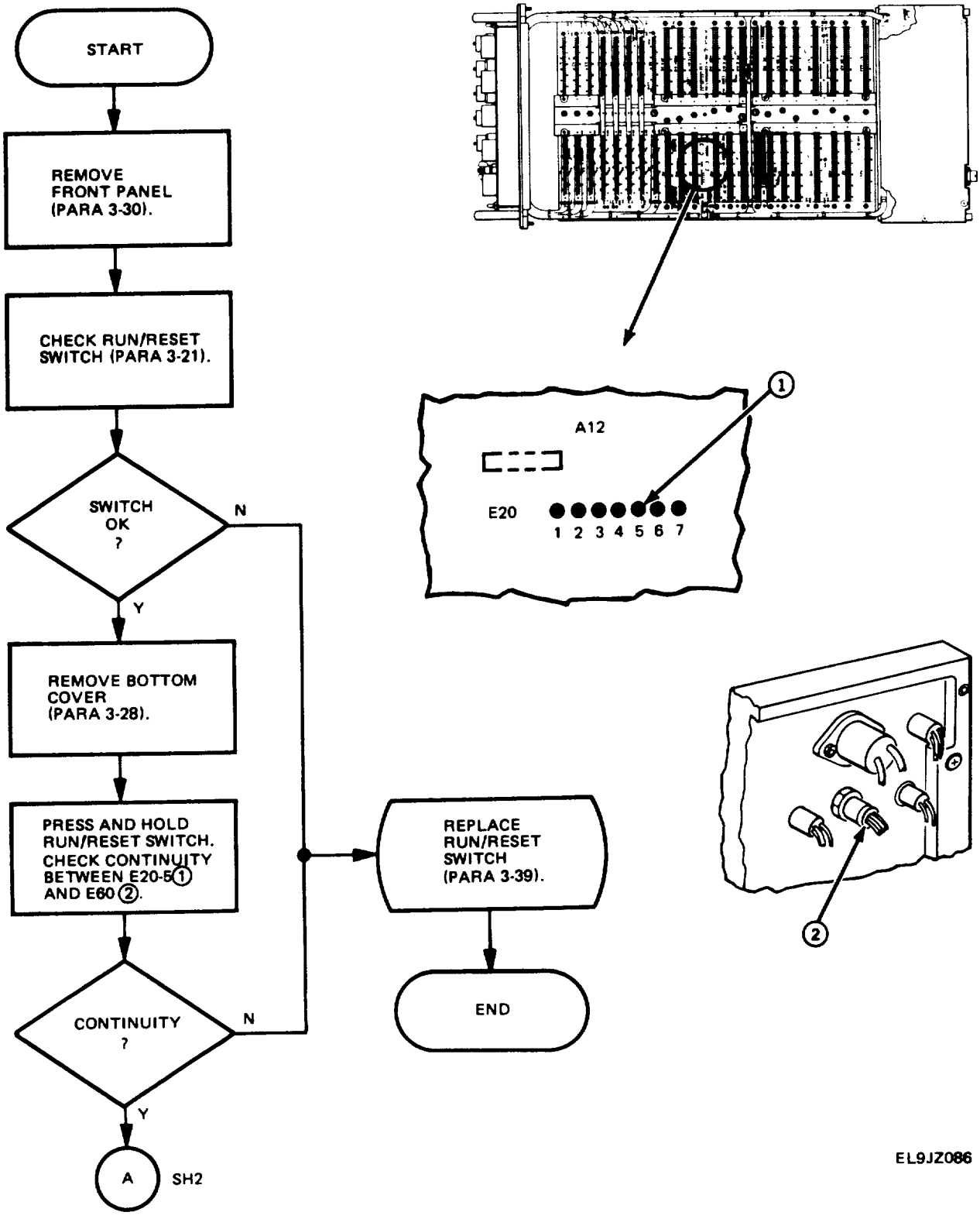
TROUBLESHOOTING FLOWCHART 6

BATT INDICATOR NOT LIT, SEMI MEMORY (SHEET 13 OF 13)



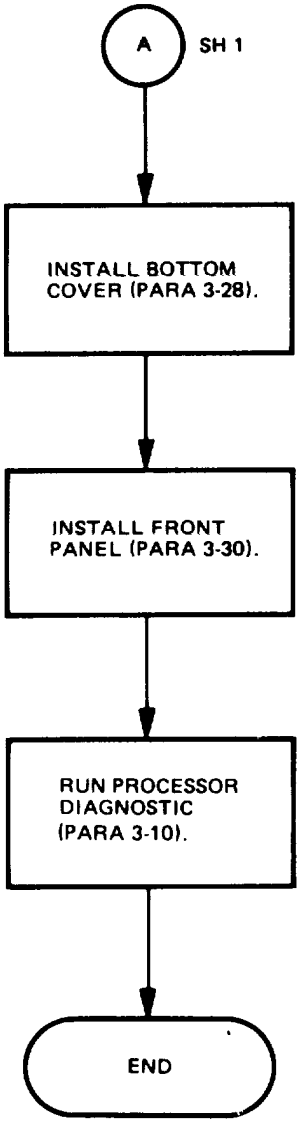
TROUBLESHOOTING FLOWCHART 7

RUN/RESET INDICATOR WON'T LIGHT, CORE MEMORY (SHEET 1 OF 2)



TROUBLESHOOTING FLOWCHART 7

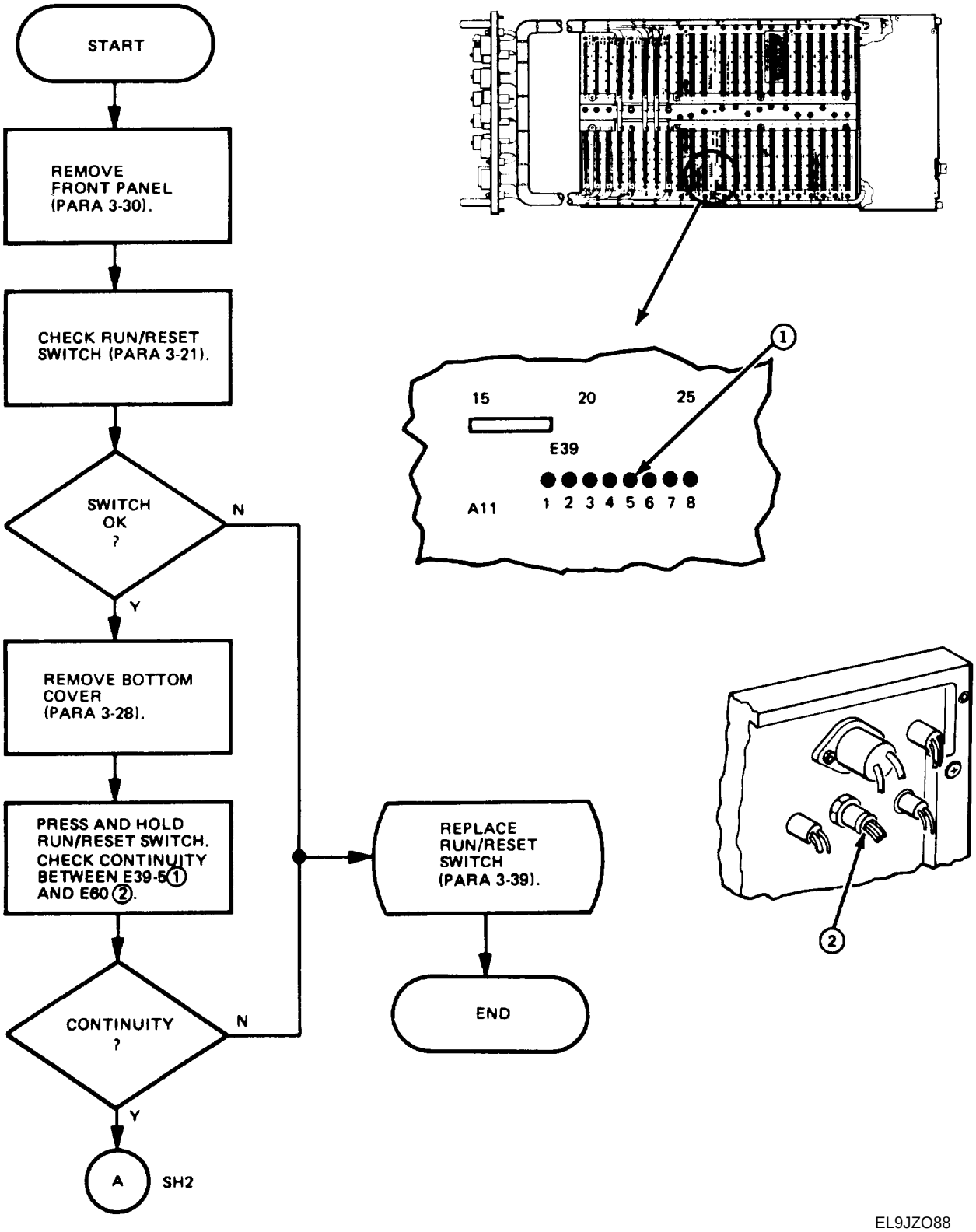
RUN/RESET INDICATOR WON'T LIGHT, CORE MEMORY (SHEET 2 OF 2)



EL9JZ087

TROUBLESHOOTING FLOWCHART 8

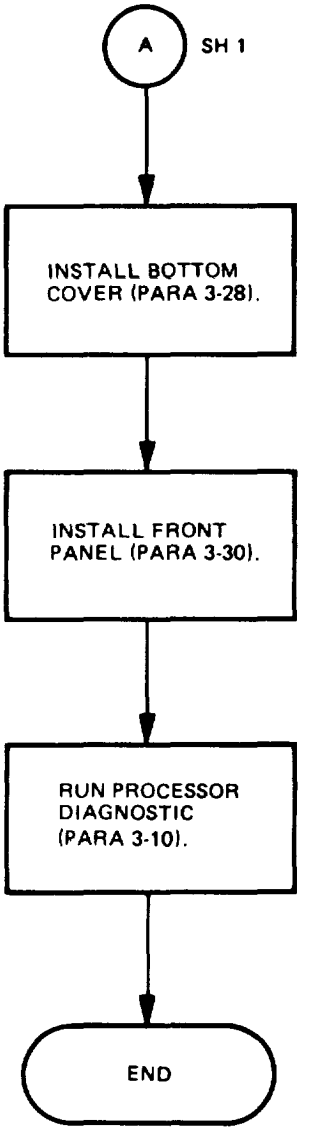
RUN/RESET INDICATOR WON'T LIGHT, SEMI MEMORY (SHEET 1 OF 2)



EL9JZO88

TROUBLESHOOTING FLOWCHART 8

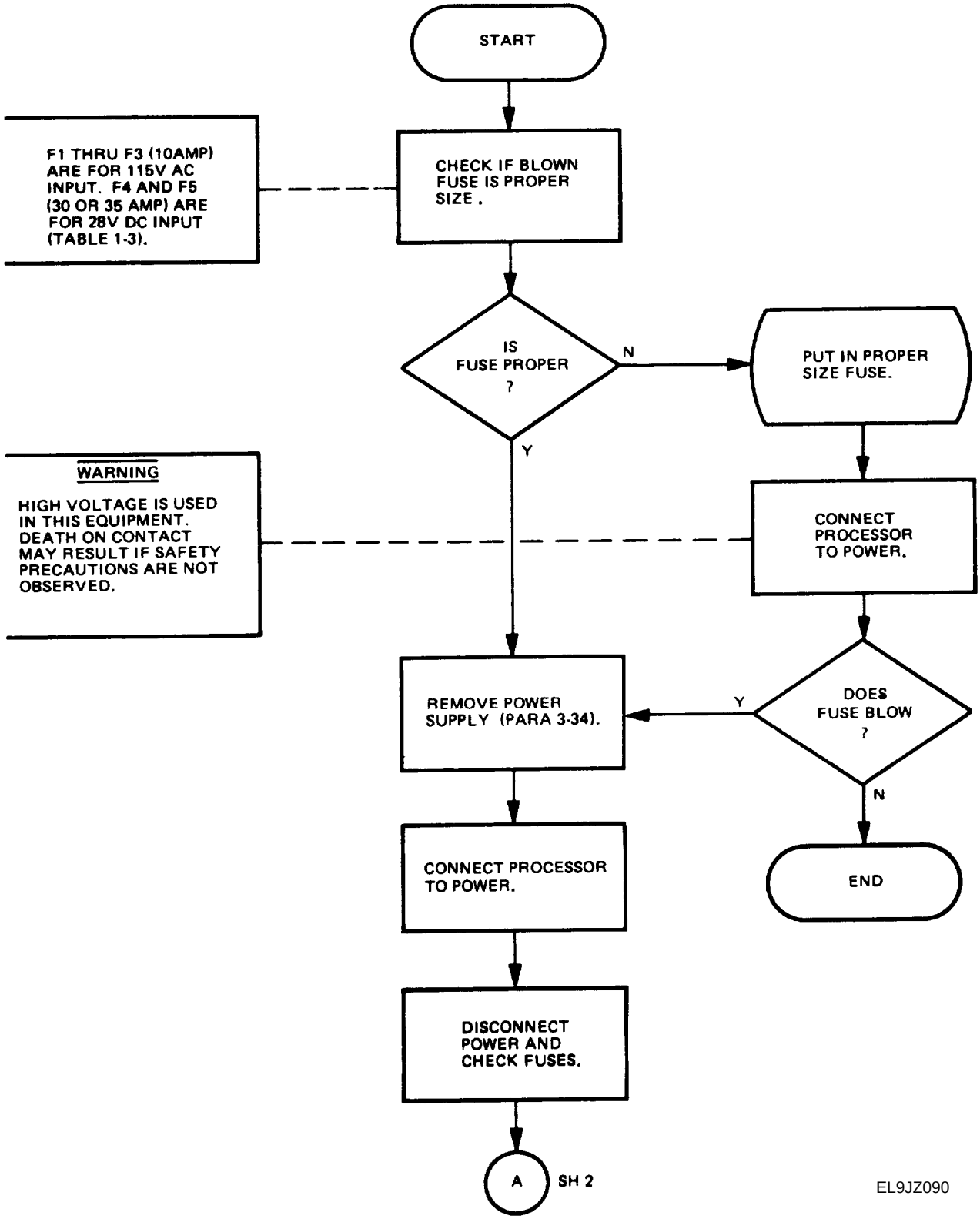
RUN/RESET INDICATOR WON'T LIGHT, SEMI MEMORY (SHEET 2 OF 2)



EL9JZ089

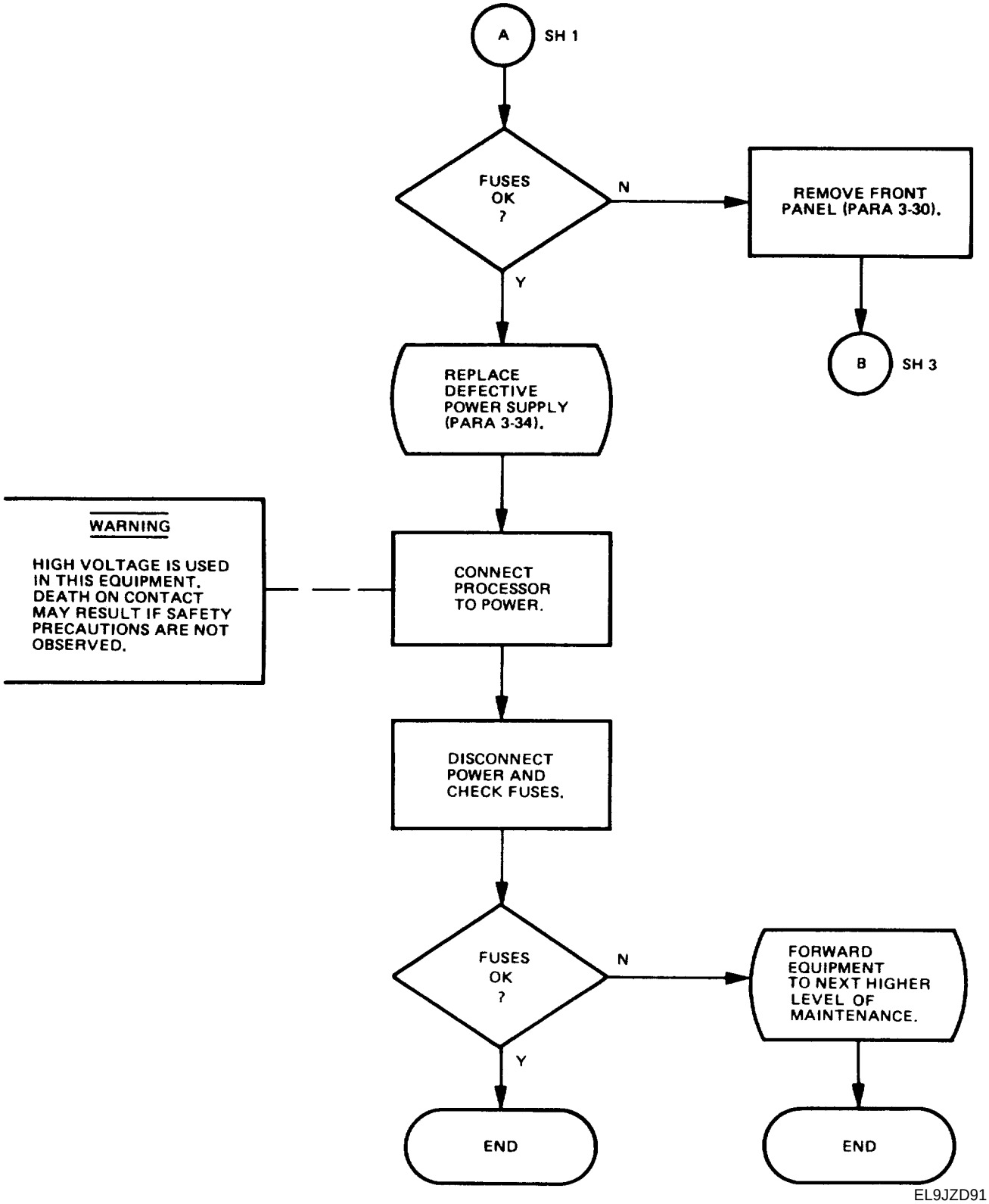
TROUBLESHOOTING FLOWCHART 9

PROCESSOR KEEPS BLOWING FUSES (SHEET 1 OF 6)



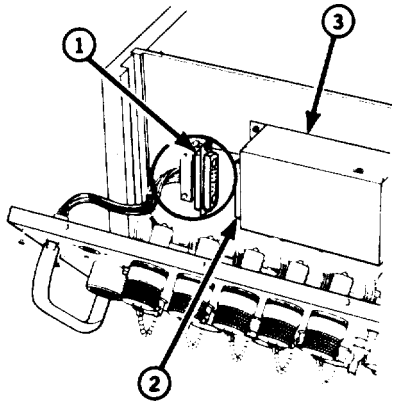
TROUBLESHOOTING FLOWCHART 9

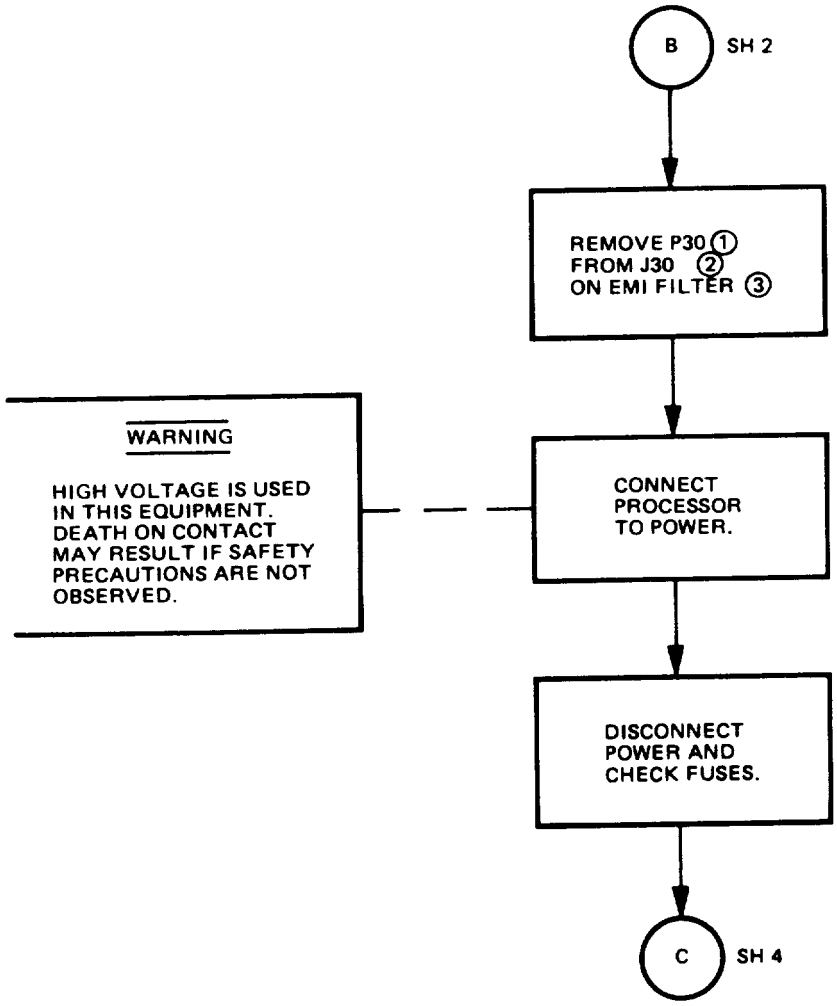
PROCESSOR KEEPS BLOWING FUSES (SHEET 2 OF 6)



TROUBLESHOOTING FLOWCHART 9

PROCESSOR KEEPS BLOWING FUSES (SHEET 3 OF 6)

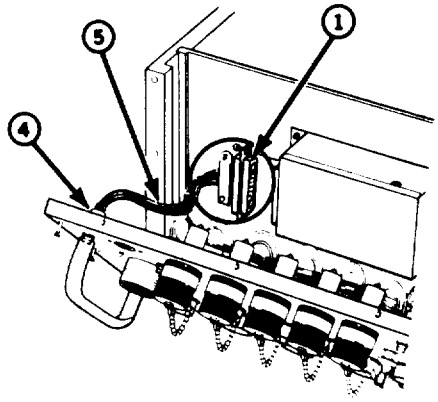




EL9JZ092

TROUBLESHOOTING FLOWCHART 9

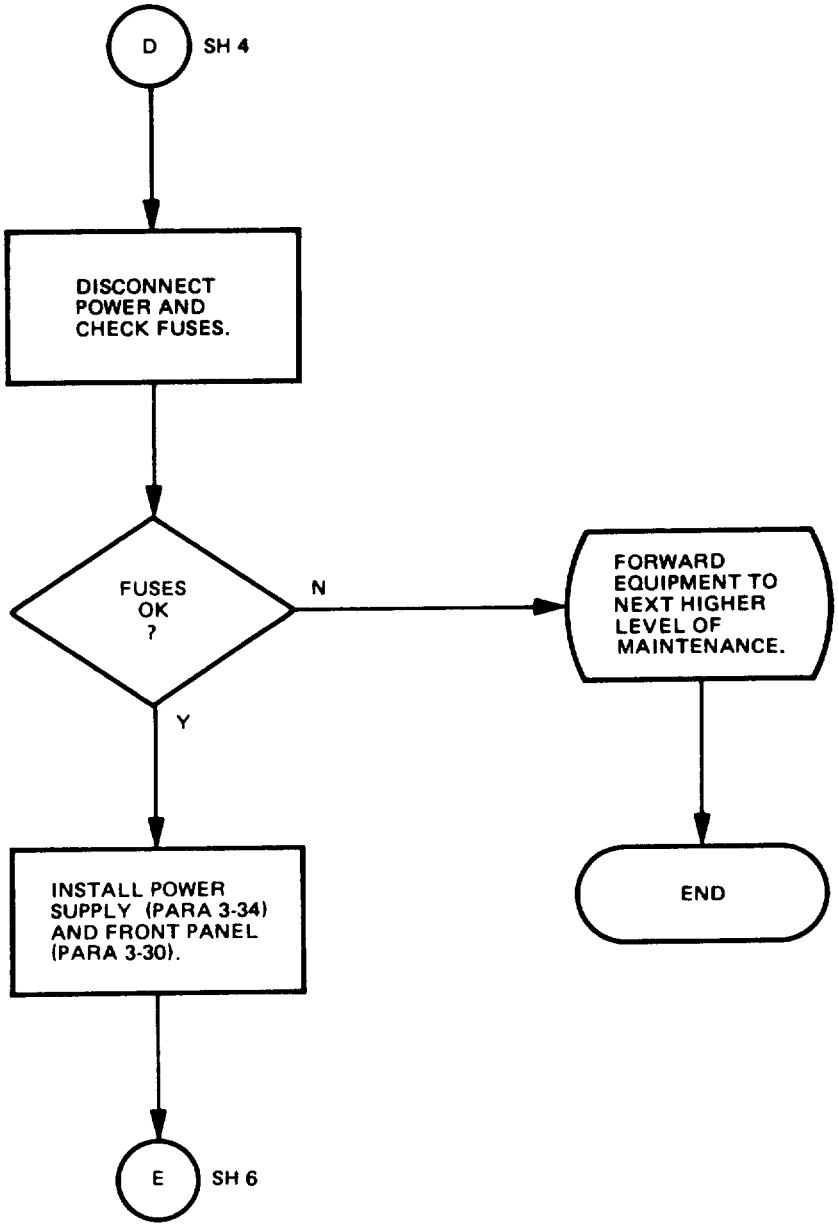
PROCESSOR KEEPS BLOWING FUSES (SHEET 4 OF 6)



EL9JZ093

TROUBLESHOOTING FLOWCHART 9

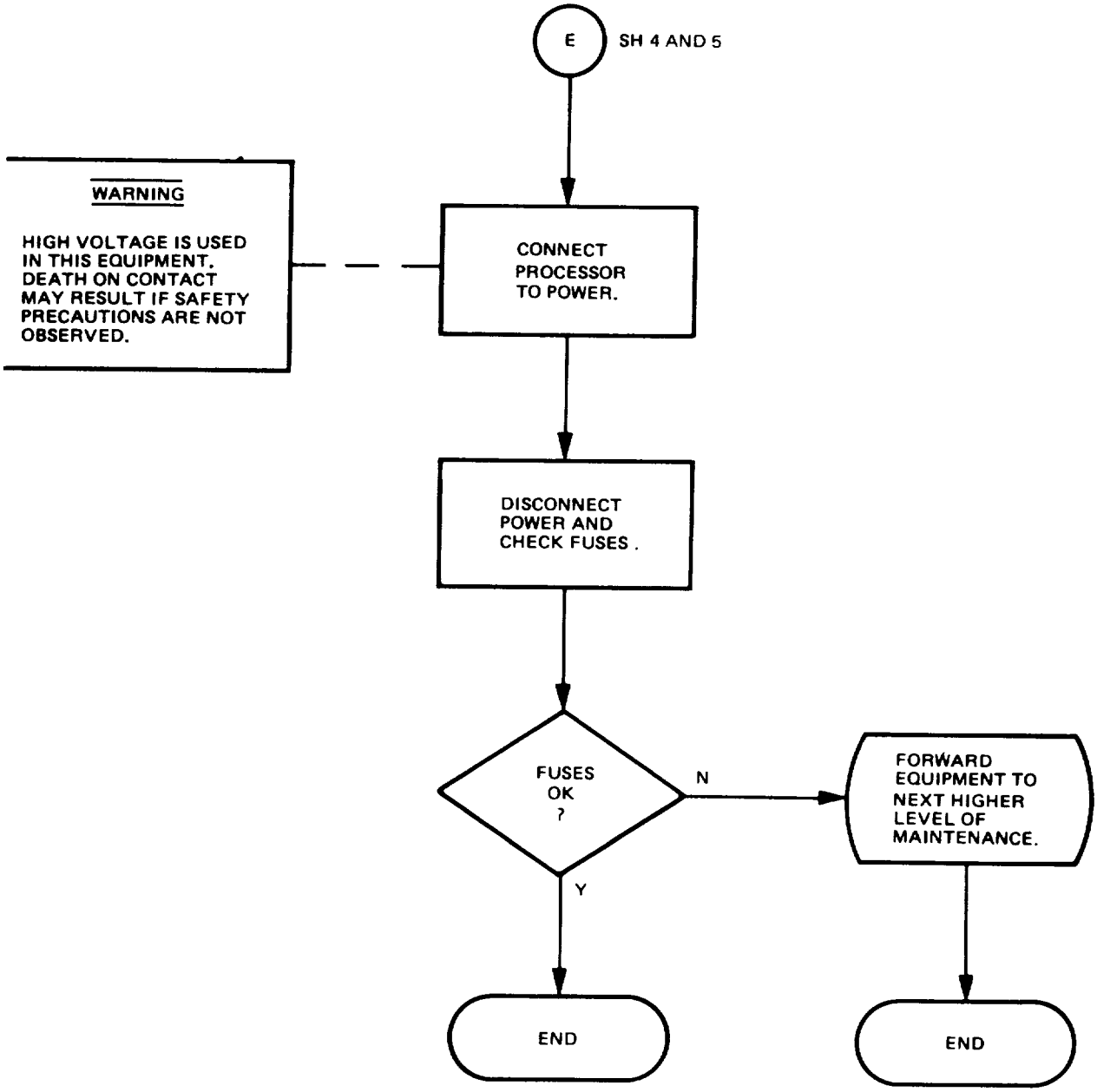
PROCESSOR KEEPS BLOWING FUSES (SHEET 5 OF 6)



EL9JZ094

TROUBLESHOOTING FLOWCHART 9

PROCESSOR KEEPS BLOWING FUSES (SHEET 6 OF 6)



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The second serving step is to trace the fault to a particular module or major component within the assembly or subassembly (e.g., power rectifying section, clock circuitry, connector, etc.). This is called LOCALIZATION. Continued checking and testing for the fault narrows the problem to the module or major component.

The final step in the troubleshooting process is to trace the fault to a defective component within the identified module or major component (e.g., resistor, wire, chip, pin, etc.). This is called ISOLATION.

NOTE

Fault isolation, in most cases, is beyond the scope of direct support maintenance. Such isolation, and the required repair activity, is accomplished at either the SRA or depot maintenance facilities.

Localization and isolation of a fault(s) is normally determined by visual inspection, voltage and resistance measurements, the use of troubleshooting flowcharts, and the running of diagnostics. Visual inspection will locate and isolate many faults (e.g., burnt out light-emitting diode (LED), loose connector, blown fuse, etc.), without testing the circuits. Once it has become obvious that a fault does exist in the operational performance of the processor, a visual inspection for faults is conducted prior to going into the testing of circuits.

NOTE

When performing checks and tests to locate equipment fault(s), consider intermittent faults as a contributing factor. Jarring or tapping the equipment, or jiggling a wire or component could expose this type of problem.

The objective of direct support maintenance troubleshooting is the localization of a fault to a defective assembly, subassembly, chassis mounted component, or the chassis itself. Use the troubleshooting flowcharts (para 3-7) and the procedures to localize and aid faults.

The first step in troubleshooting the processor is to locate the symptom in the troubleshooting symptom index (table 3-5). Next, go to the applicable flowchart or procedure for that symptom. After performing the required troubleshooting and making repairs, observe that upon application of power to the processor that the BITE self-test is completed successfully, ensuring that repairs have been accomplished properly.

The following general rules apply while performing troubleshooting:

1. Follow the troubleshooting flowcharts and procedures in the order indicated by the flow arrows or sequence of procedural steps.

2. Perform only one instruction at a time.

3. Start at the beginning of the troubleshooting flowchart or procedure. Do not start in the middle.

4. When making repairs, replacing components, or performing continuity checks, always shut off power to the equipment unless specified otherwise in the applicable repair procedure.

5. When measuring voltages, current, or waveforms, ensure that the processor and all test equipment are properly grounded. Observe high voltage warnings listed on the warning page at the front of this manual.

a. Smoke and Fire. A unit received from organizational maintenance tagged as smoke or fire damaged will be thoroughly checked over by direct support maintenance personnel, and as required, be serviced/repaired and returned to service or forwarded to higher levels of maintenance.

NOTE

In cases of smoke and fire damage, direct support maintenance is limited to the replacement of the PCBs, power supply, EMI filter, or fuse assemblies. All other repair activities are referred to higher levels of maintenance.

Following is a step-by-step procedure for servicing and repairing a smoke or fire damaged processor.

(1) Review the documents (tag, forms, etc.) that accompanied the defective unit received from organizational maintenance.

(2) Make a visual inspection of the unit and endeavor to determine if the unit is serviceable at this level.

(3) If the processor's external surfaces have been smoke and fire damaged, refer the unit directly to depot maintenance for chassis overhaul and unit operational checkout.

NOTE

Most smoke and fire malfunctions within a processor are likely to occur in the power section. Seldom will there be smoke or fire malfunctions in the other sections due to the circuit shutdown features of the power supply and the ac and dc fusing in the power circuitry.

(4) Unless otherwise indicated by smoke c. burn marks at the front of the processor, remove the unit's power supply (para 3-33).

(5) Once the power supply has been removed from the processor, visually inspect it for signs of damage, without attempting any disassembly of the power supply.
HINT: Inspect the blower fan closely.

(6) if it is obvious that the damage is confined totally to the power supply, forward the defective supply directly to the depot maintenance facilities for repair. Replace the defective supply with an operational unit from spares. Proceed to procedural step (11).

(7) If there is damage in the power supply but it does not appear to be confined to the power supply (i.e., connector J14/P14, J15/P15, or J17/P17 show signs of overheating or burning) forward the processor to the next higher level of maintenance.

(8) If the power supply doesn't appear to be the problem, open the front panel to expose the EMI filter and panel wiring (para 3-34).

(9) Visually inspect the EMI filter, its connectors and wiring. If the problem is in the filter itself with no signs of damaged wiring or connectors, replace the filter (para 3-34) with an operational spare. Proceed to step (11) to follow.

(10) If the problem was not in the EM I filter or the power supply, make a careful inspection of the fuses at the rear of the front panel (para 3-35). Check for shorted wiring, burnt fuse housing, etc.

(11) If a fuse assembly has been burned, remove and replace the defective component (para 3-35).

(12) If steps (5), (8), or (10) corrected the problem, perform the processor testing per paragraph 3-12.

(13) If the action taken to this point in the process has not corrected the malfunction, or if the cause of the malfunction cannot be located and isolated, forward the defective processor to the next higher level of maintenance.

b. Unit Overheating. A unit received from organizational maintenance tagged as having an overheating problem is only partially serviceable at direct support. If the blower fan is defective, the blower fan is replaced (para 3-32). If an air duct is clogged or damaged, remove the air duct and unclog or replace (para 3-30). If there appears to be other cause of the overheating problem, replace the power supply (para 3-3) and test the processor in accordance with paragraph 3-12.

c. Noisy Blower Fan. If a unit is received with a tag identifying the problem as a noisy blower fan, replace the fan in accordance with paragraph 3-32 and return the unit to service.

d. Defective Power Cable. Refer to paragraph 3-16 for testing procedure and paragraph 3-46 for repair procedure.

e. Defective Battery Power Cable. Refer to paragraph 3-16 for testing procedure and paragraph 3-46 for repair procedure.

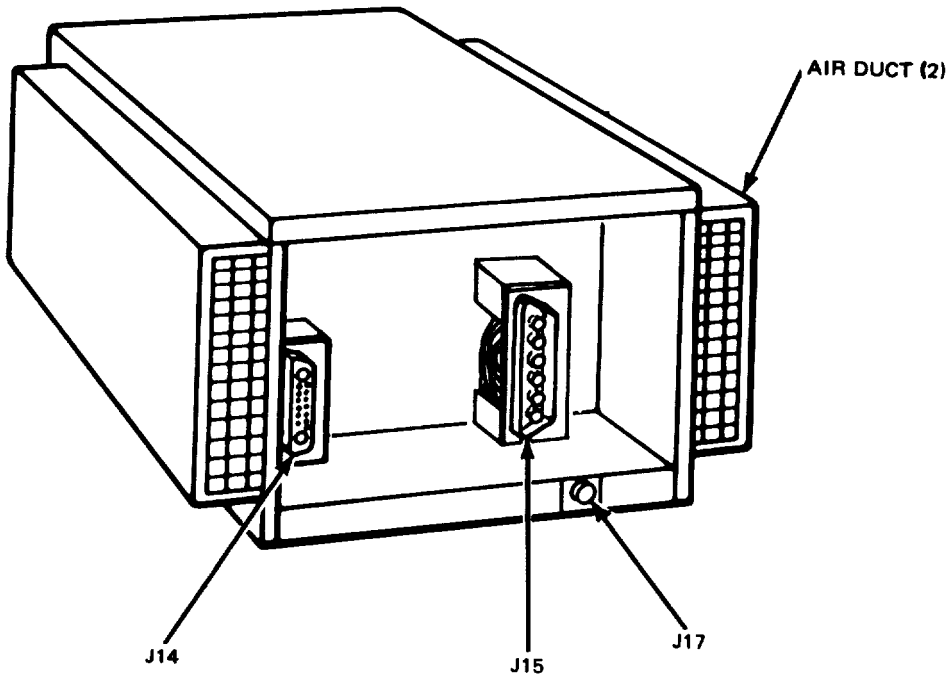

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Figure 3-5. Chassis Connectors for the Power Supply

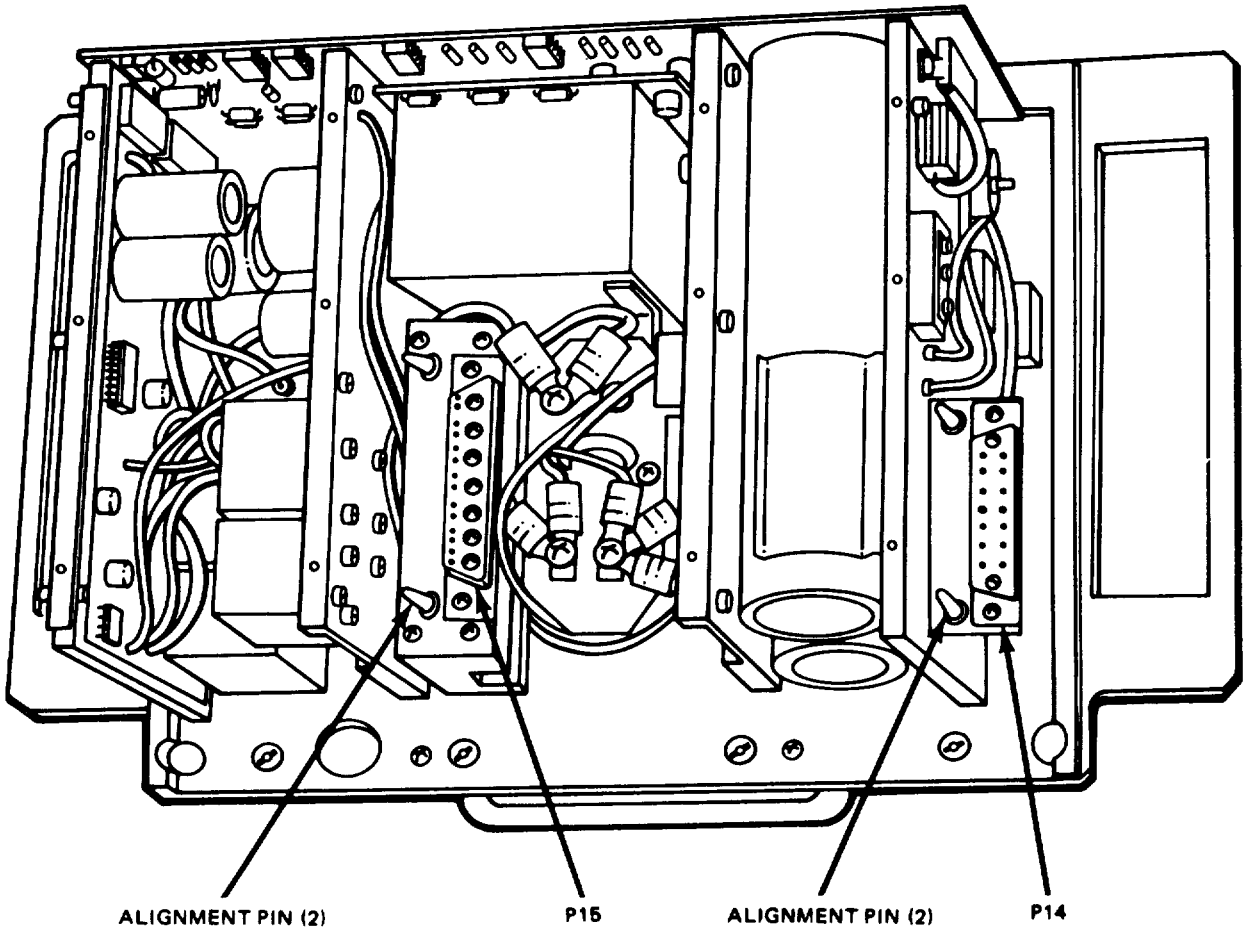

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Figure 3-6. Model 5617 Power Supply (AC), Component View

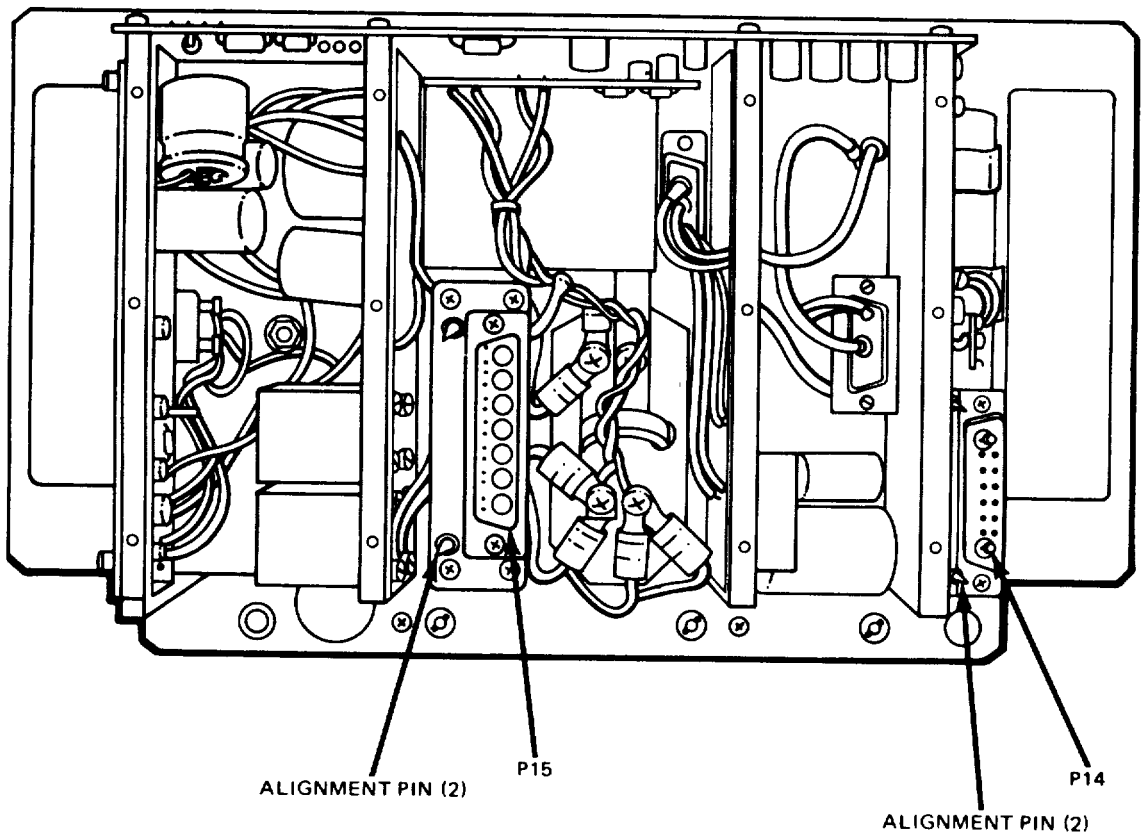


Figure 3-7. Model 5687 Power Supply (DC), Component View

f. Defective I/O Cable. Refer to paragraph 3-17 for testing procedure and paragraph 3-45 for repair procedure.

g. Defective ETM indicator. Refer to paragraph 3-19 for testing procedure and paragraph 3-37 for replacement procedure.

h. Program Won't Load. Run the diagnostics procedures (para 3-10).

i. Processor Does Not Accept Data. Run the diagnostics procedures (para 3-10).

j. Process Does Not Output Data. Run the diagnostics procedures (para 3-10).

3-10. DIAGNOSTIC PROCEDURES

Following this page are the maintenance diagnostics procedures in flowchart form. The diagnostics are used during troubleshooting and upon the completion of repairs to the processor. This is to ensure that repairs have been accomplished property and the processor is ready to operate.

The following general rules apply while performing the diagnostics procedures:

1. Follow the flowchart and any referenced test, repair, or replacement procedures in the order indicated by the flow arrows or sequence of procedural steps.

2. Perform only one instruction at a time.

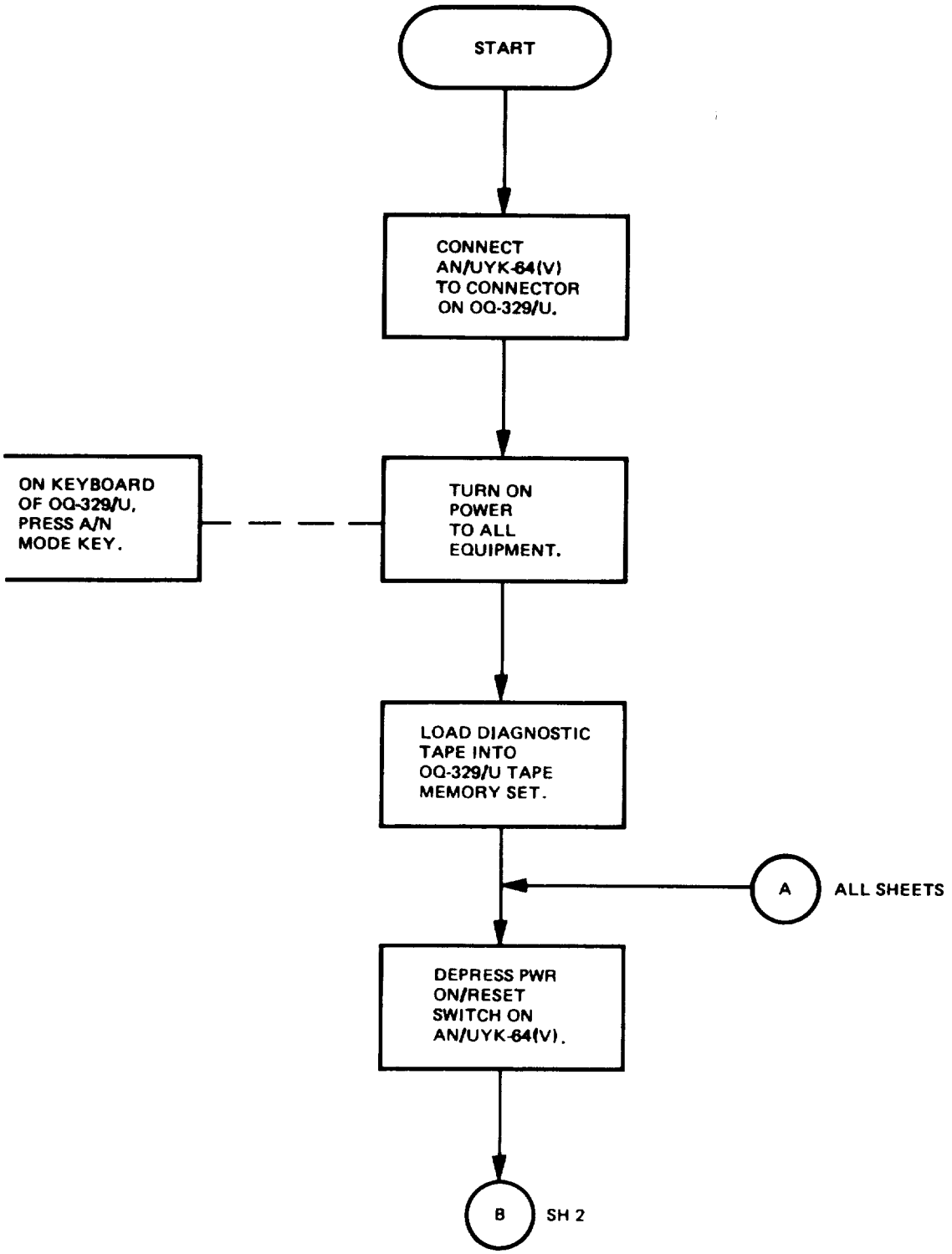
3. Start at the begining of the flowchart, and any referenced procedures. Do not start in the middle.

4. When making repairs, replacing components, or performing continuity cheeks, always shut off power to the equipment, unless otherwise specified in the applicable procedure.

5. When measuring voltages, current, or waveforms, ensure that the processor and all test equipment are property grounded. Observe high voltage warnings listed on the warning page at the front of this manual and on the equipment.

6. Configure the processor under test and the test equipment in accordance with the applicable system configuration defined in appendix C, D, and E.

MAINTENANCE DIAGNOSTICS PROCEDURES (SHEET 1 OF 9)



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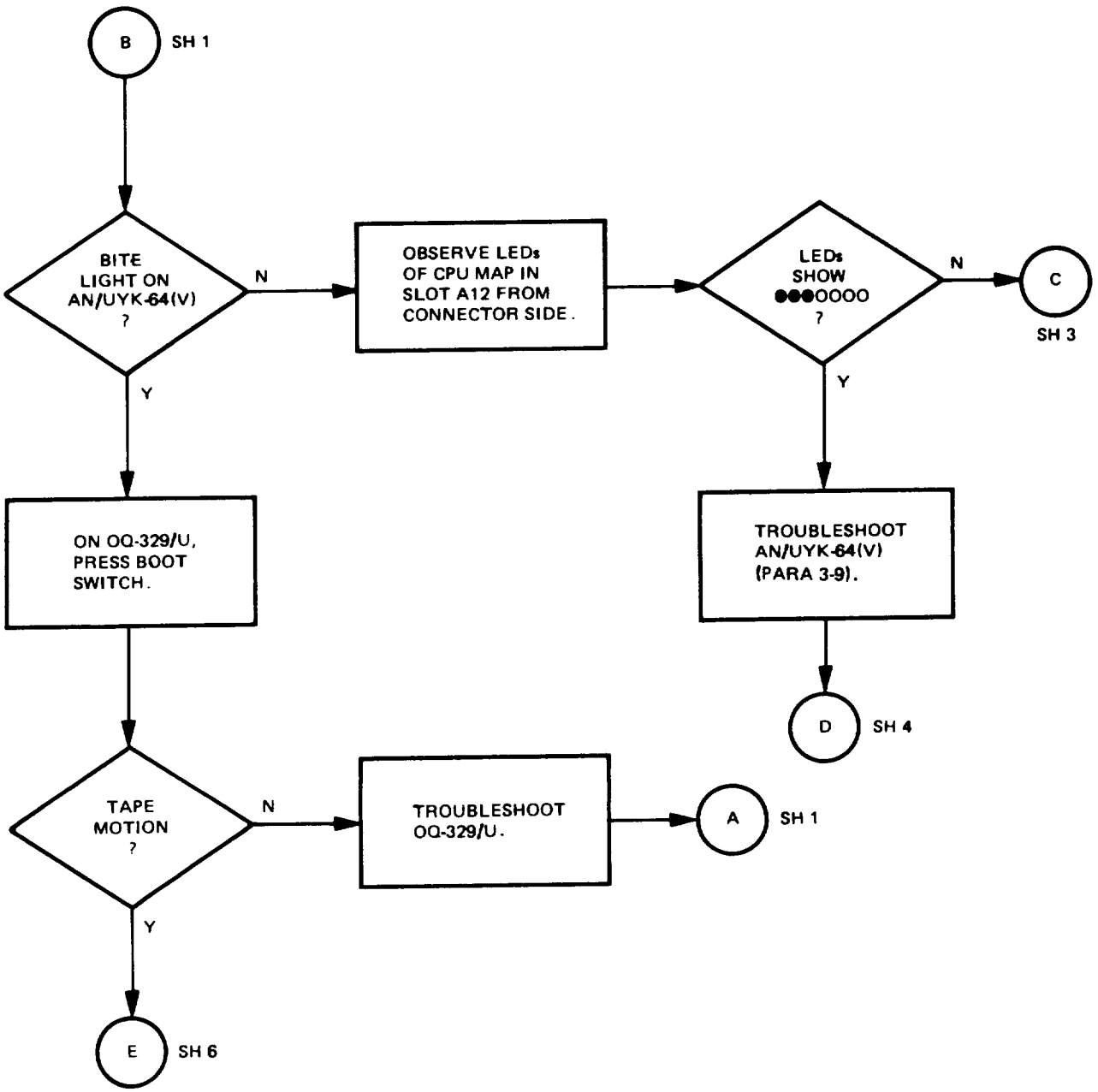
MAINTENANCE DIAGNOSTICS PROCEDURES (SHEET 2 OF 9)



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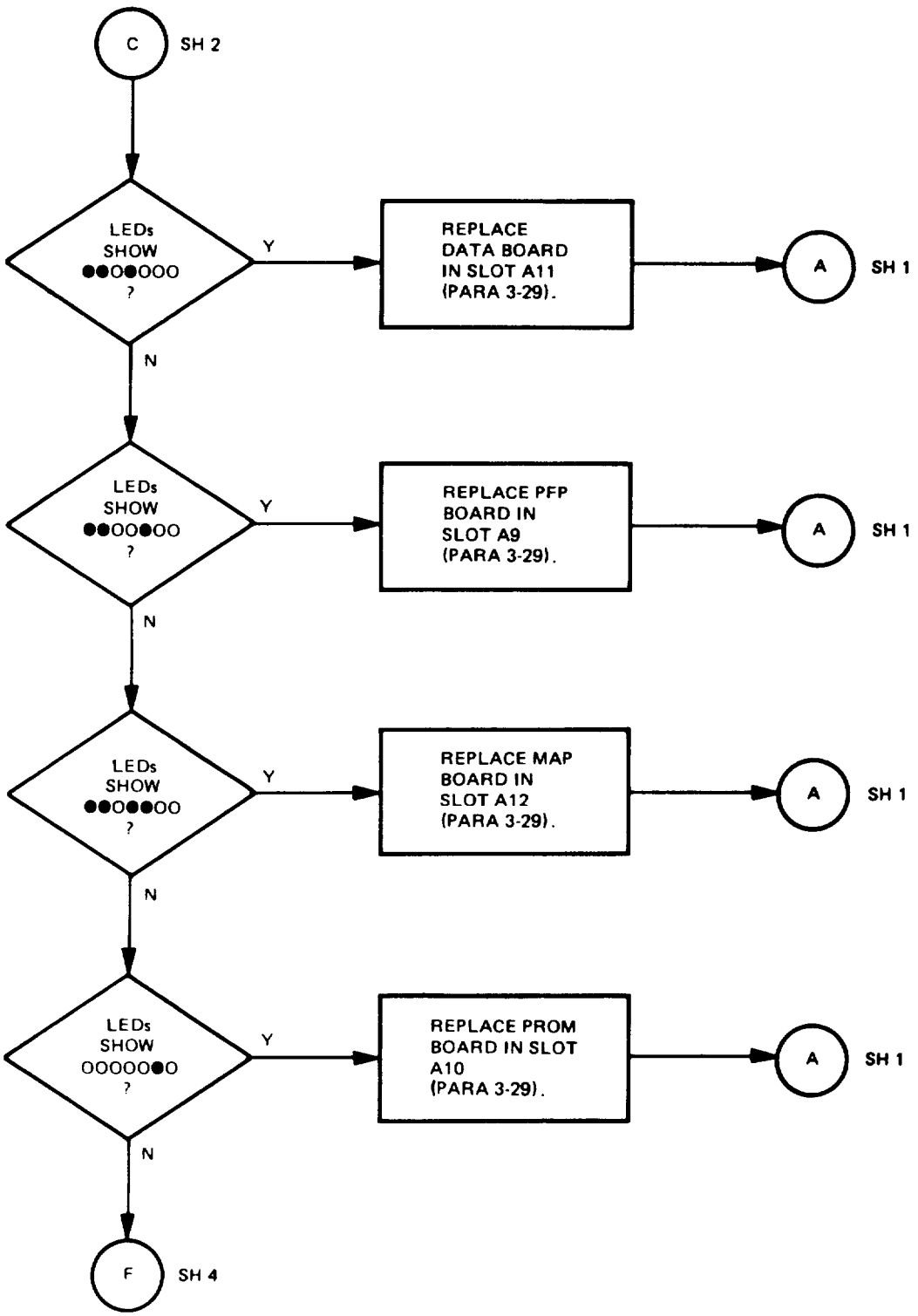
MAINTENANCE DIAGNOSTICS PROCEDURES (SHEET 3 OF 9)



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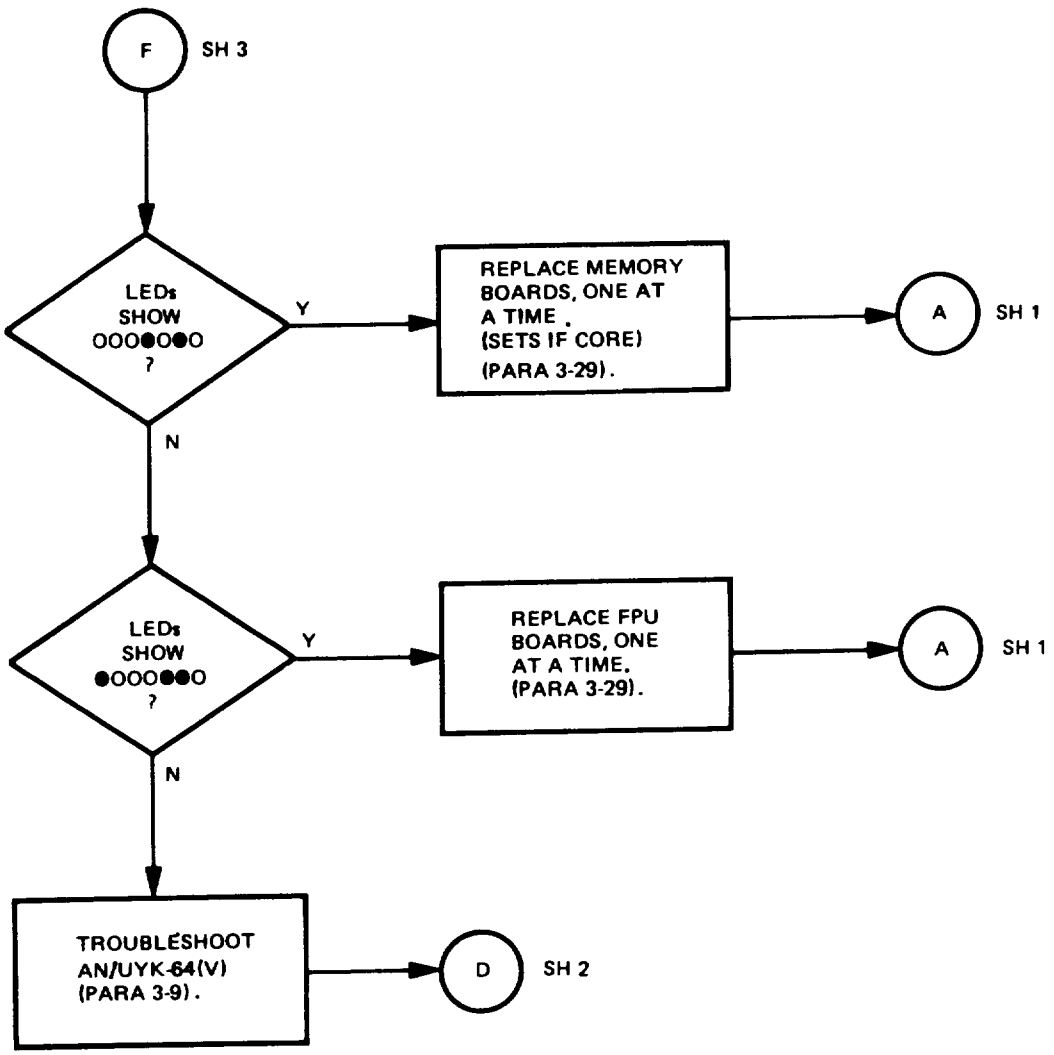
MAINTENANCE DIAGNOSTICS PROCEDURES (SHEET 4 OF 9)



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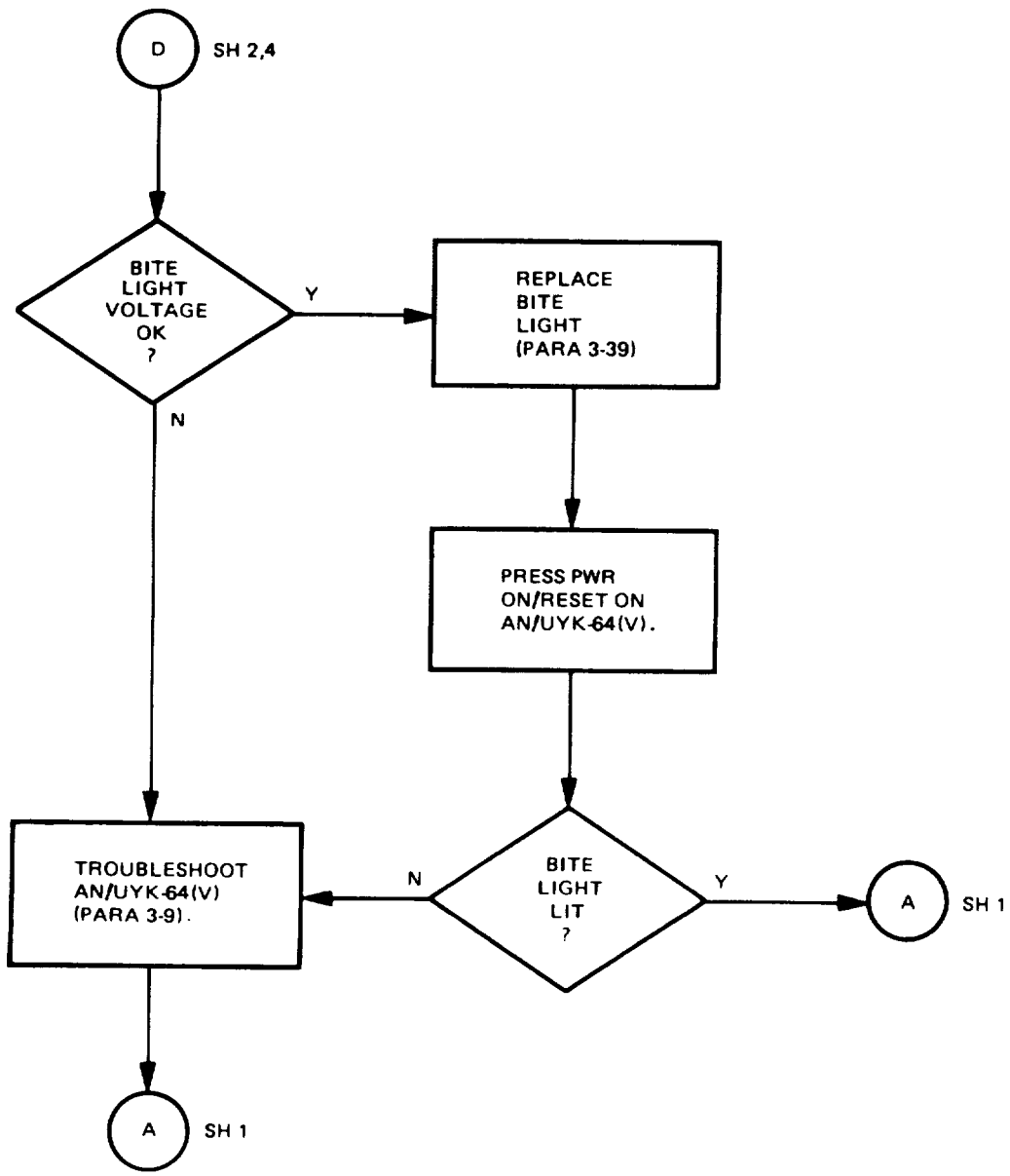
MAINTENANCE DIAGNOSTICS PROCEDURES (SHEET 5 OF 9)



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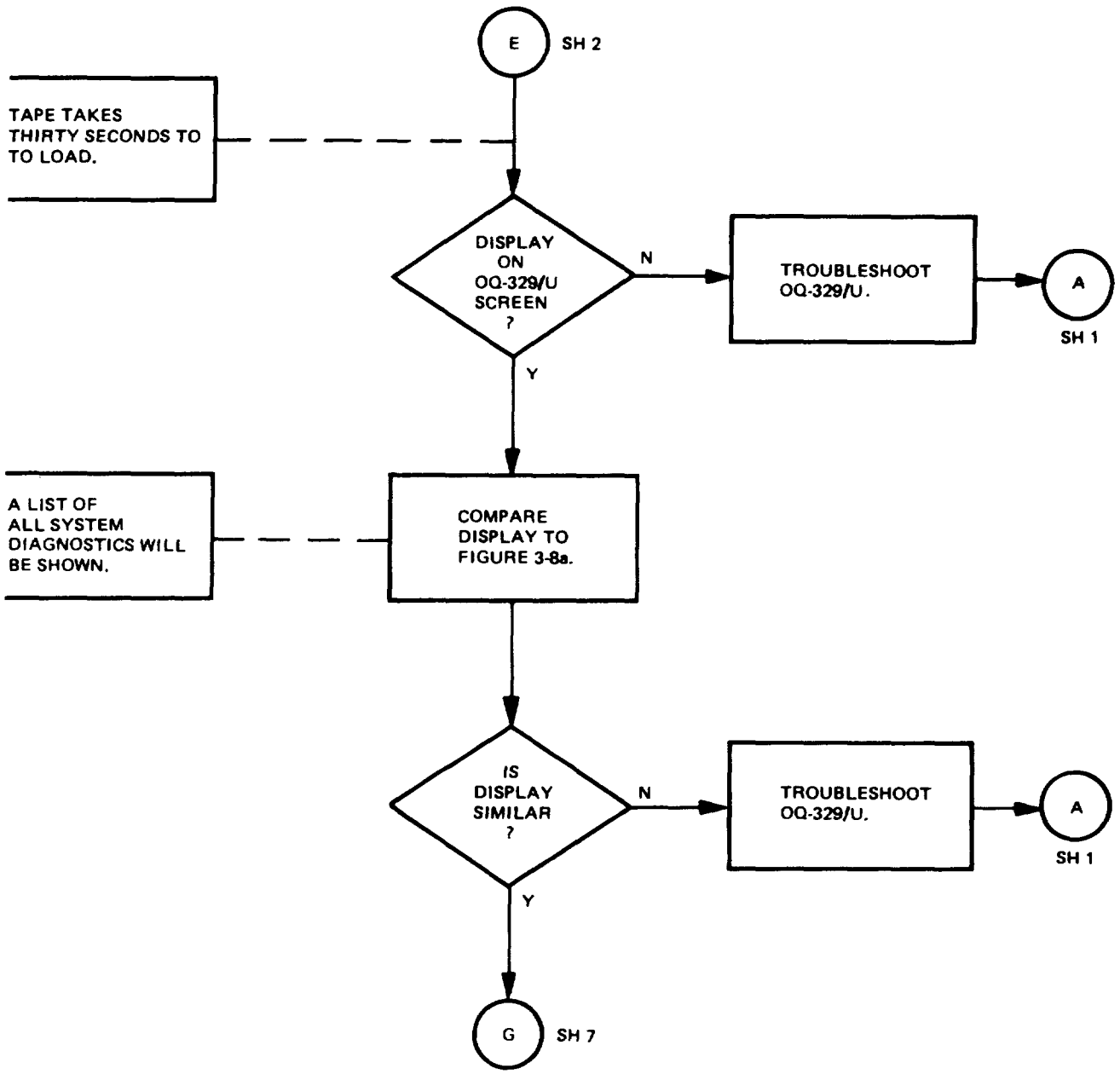
MAINTENANCE DIAGNOSTICS PROCEDURES (SHEET 6 OF 9)



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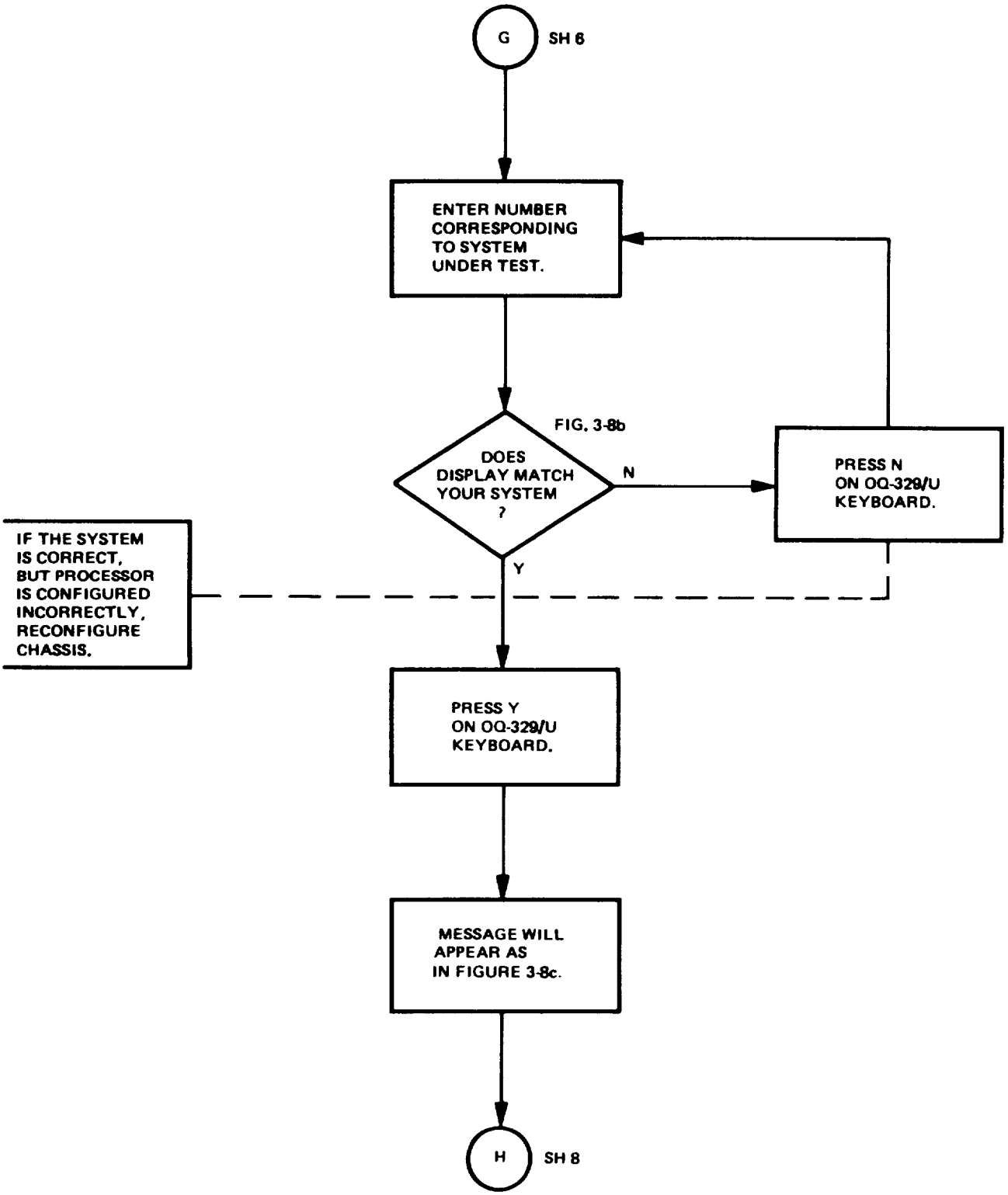
MAINTENANCE DIAGNOSTICS PROCEDURES (SHEET 7 OF 9)



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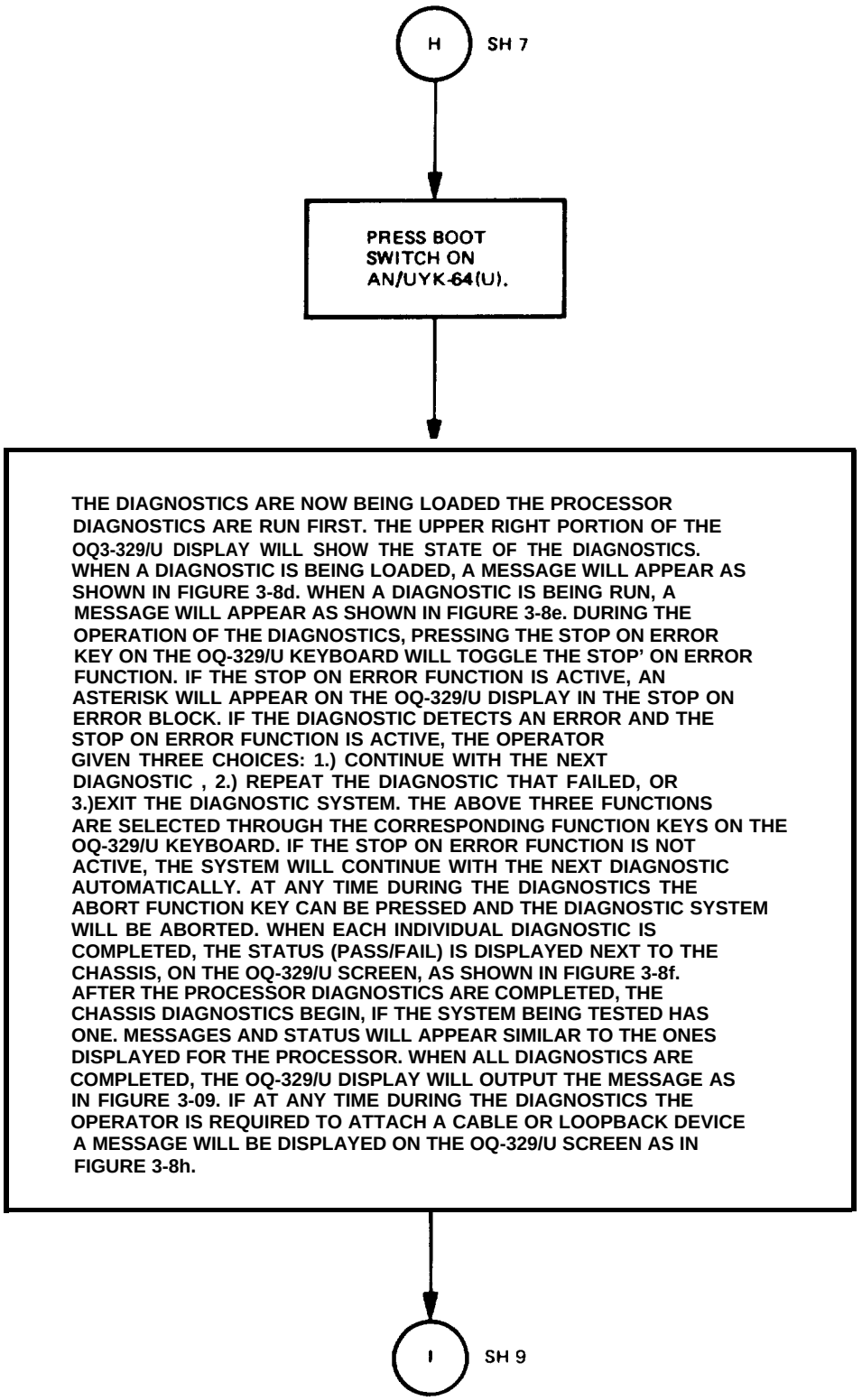
MAINTENANCE DIAGNOSTICS PROCEDURES (SHEET 8 OF 9)



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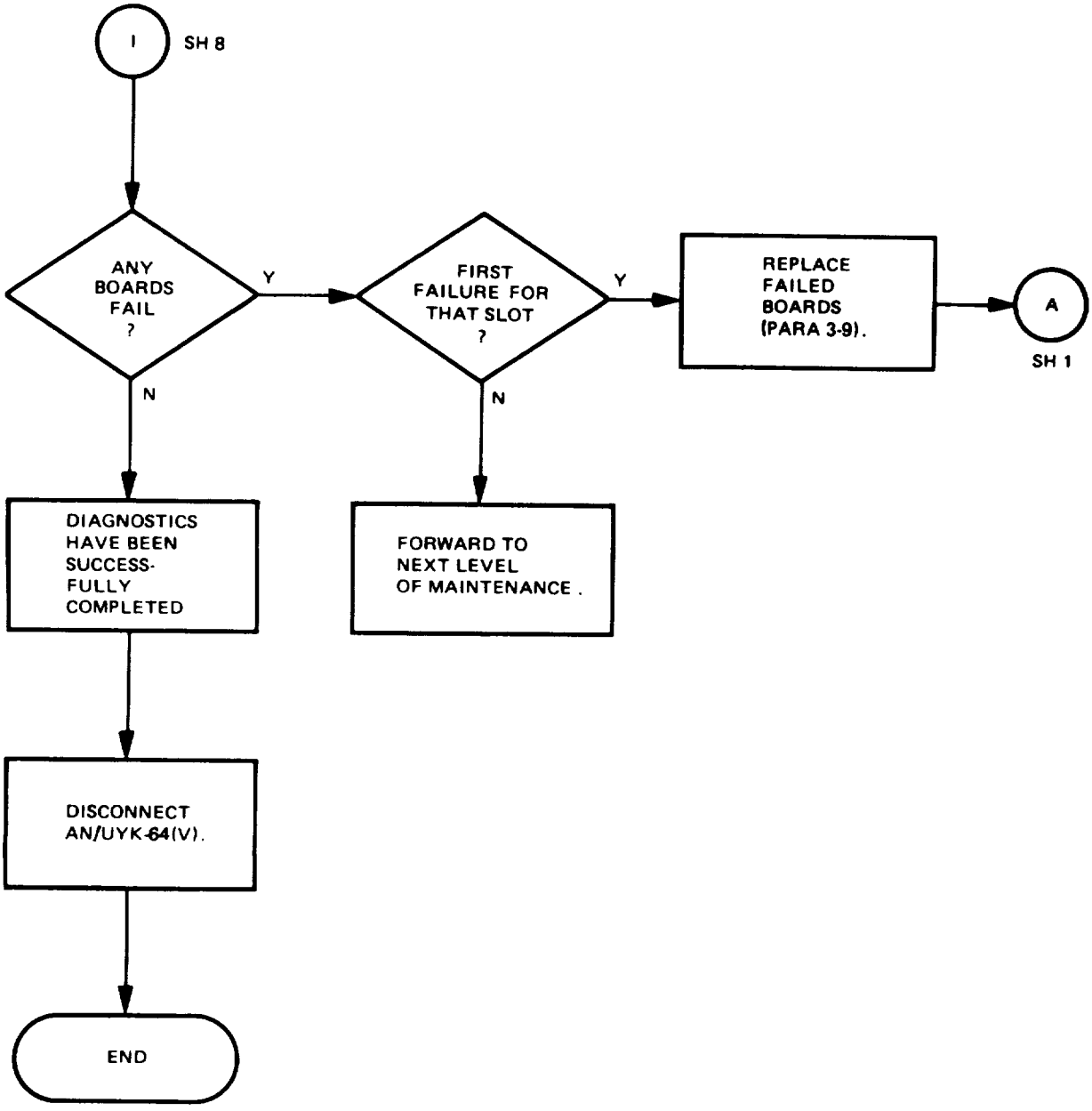
MAINTENANCE DIAGNOSTICS PROCEDURES (SHEET 9 OF 9)



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	AUTOMATED DIAGNOSTIC SYSTEM (REV 1.0)
1 - AN/MLQ-34 (TACJAM) 2 -AN/MSQ-193A (TEAMPACK) 3- AN/TMQ-31 (MDS) 4 - AN/TSC-99 RECEIVE SHELTER 5 - AN/SC-99 TRANSMIT SHELTER 6 - ANTSQ-84A SYSTEM 7 - AN/SQ-114A (TRAILBLAZER) 8 - AN/TSQ-114B (TRAILBLAZER) 9 - AN/ALQl-151 EH 1X (QUICKFIX) l0 - AN/ALQ-151 EH 60A (QUICKFIX) 11 - AN/ASN-132 INTERNAL NAVIGATION SYSTEM 12 - TT 772(P) /G DIAGNOSTIC 13 - TT 773(P) /G DIAGNOSTIC 14 - AN/UYH-1 DIAGNOSTIC 15 - AN/UYQ-10(V) DIAGNOSTIC 16 - MU 788/G DIAGNOSTIC	
SELECT SYSTEM TO BE TESTED AND PRESS CARRIAGE RETURN (CR ONLY TERMINATES THE ADS).	

EL9JZ108

Figure 3-8. Maintenance Diagnostic Display (Sheet 1 of 8)

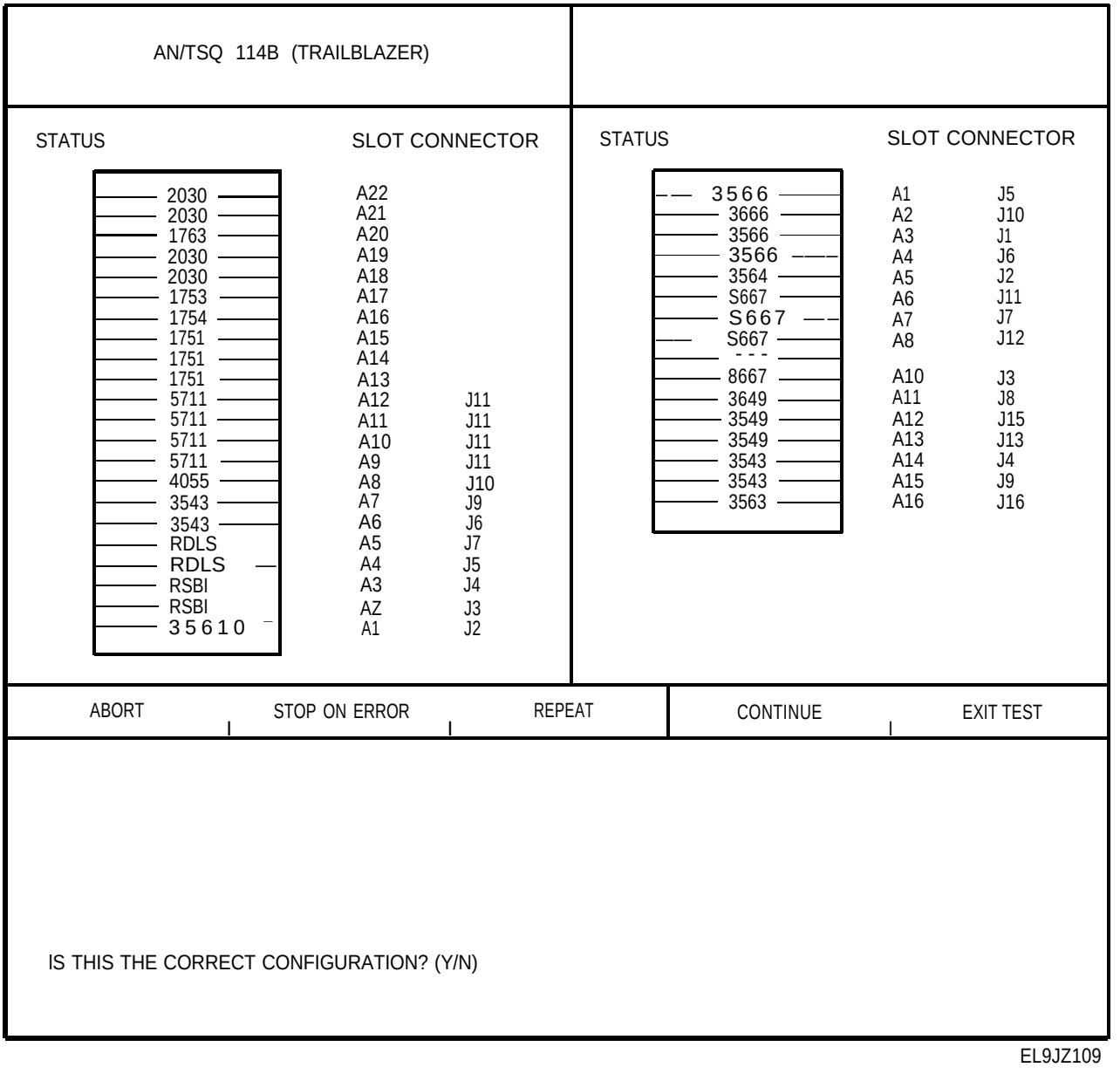

Figure 3-8. Maintenance Diagnostic Display (Sheet 2 of 8)

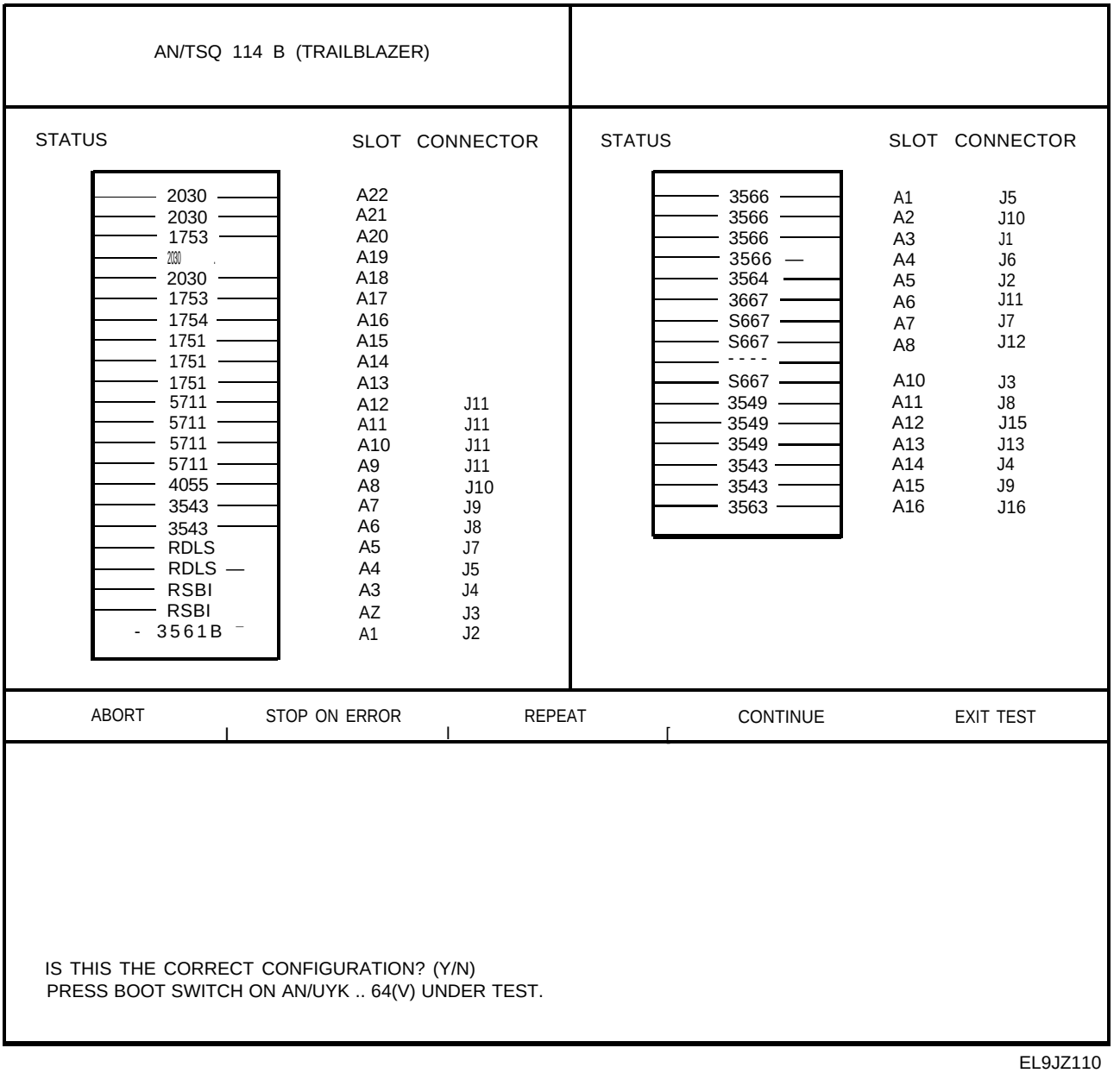

Figure 3-8. Maintenance Diagnostic Display (Sheet 3 of 8)

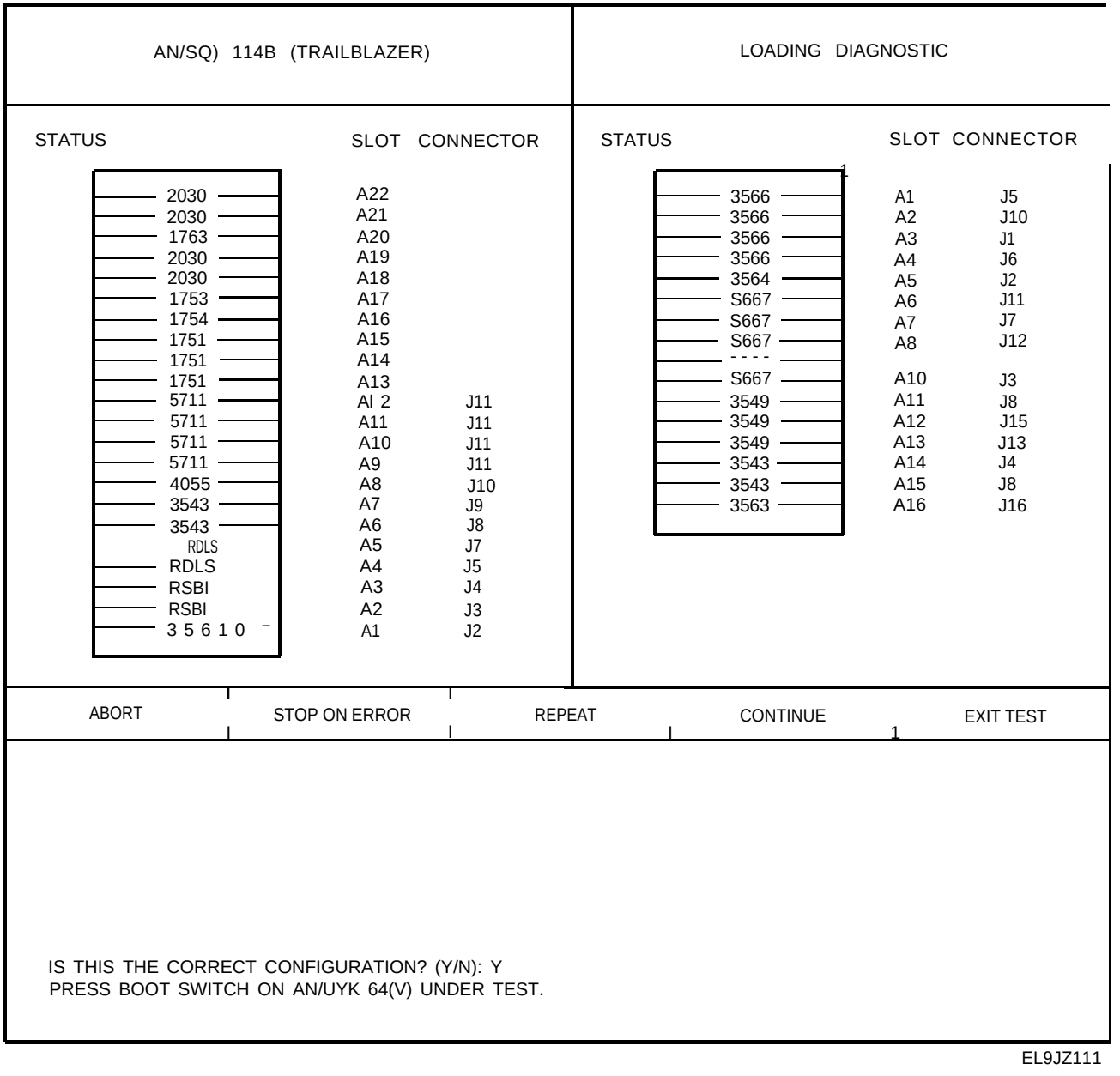

Figure 3-8. Maintenance Diagnostic Display (Sheet 4 of 8)

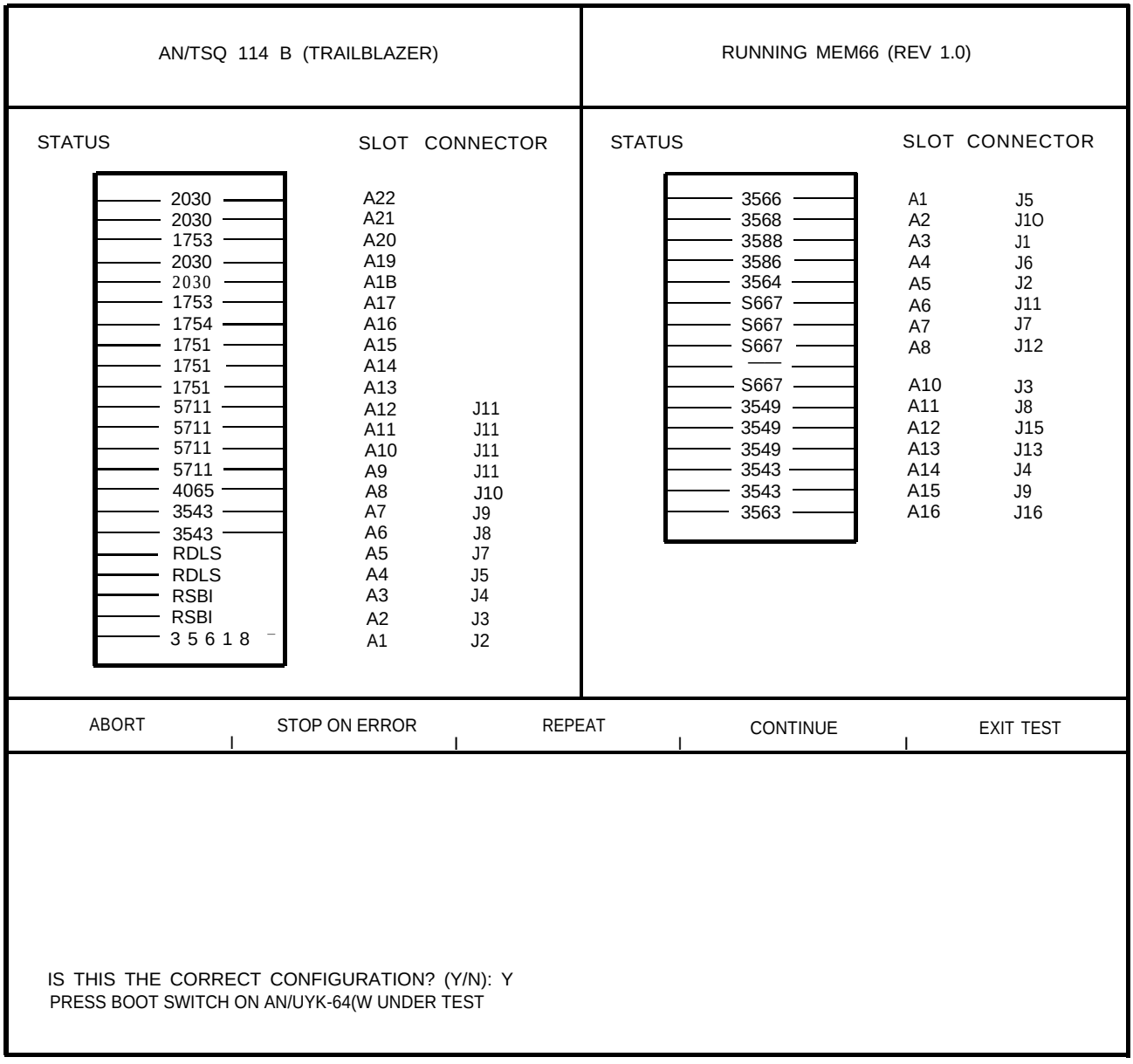

Figure 3-8. Maintenance Diagnostic Display (Sheet 5 of 8)

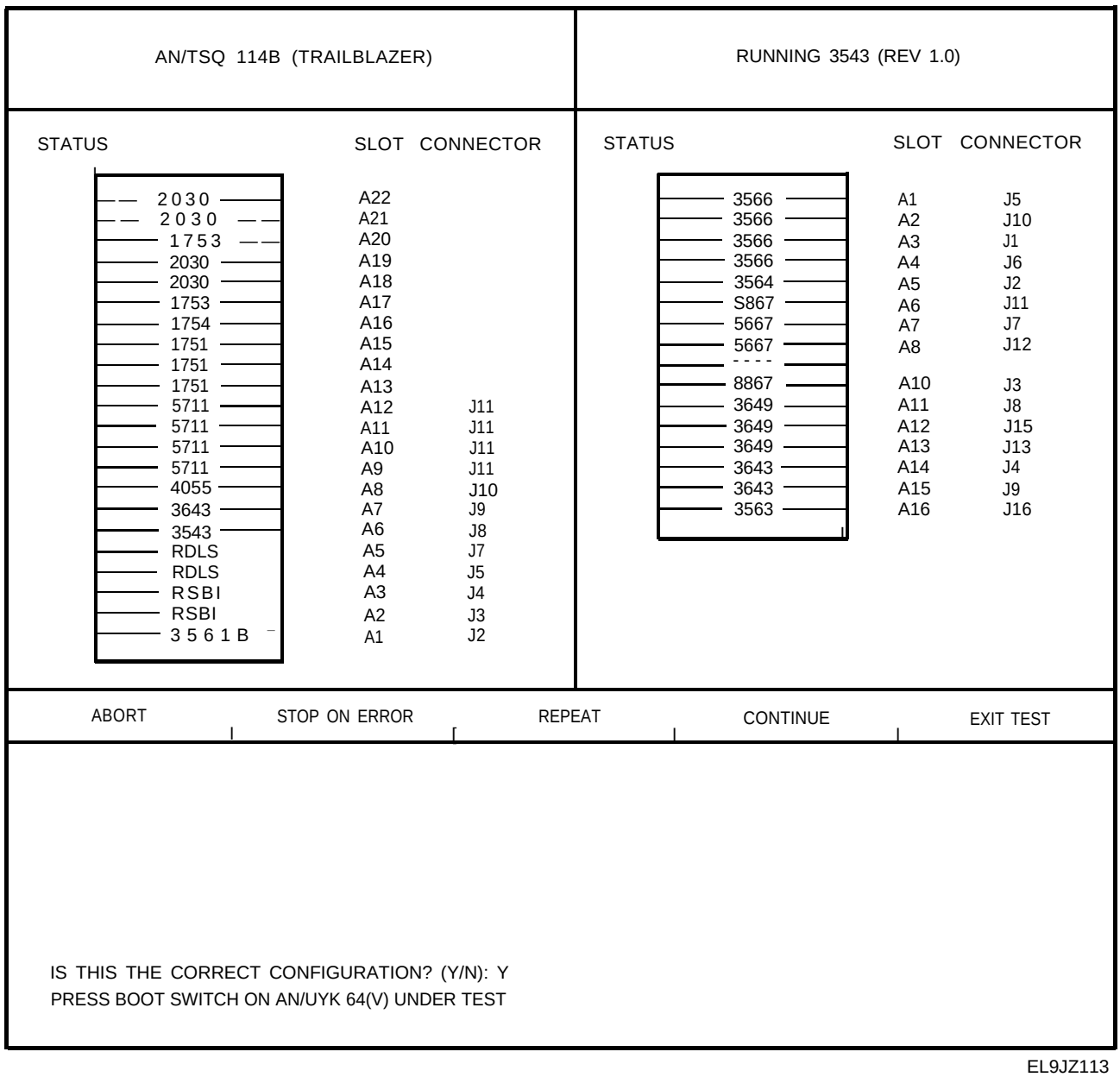

Figure 3-8. Maintenance Diagnostic Display (Sheet 6 of 8)

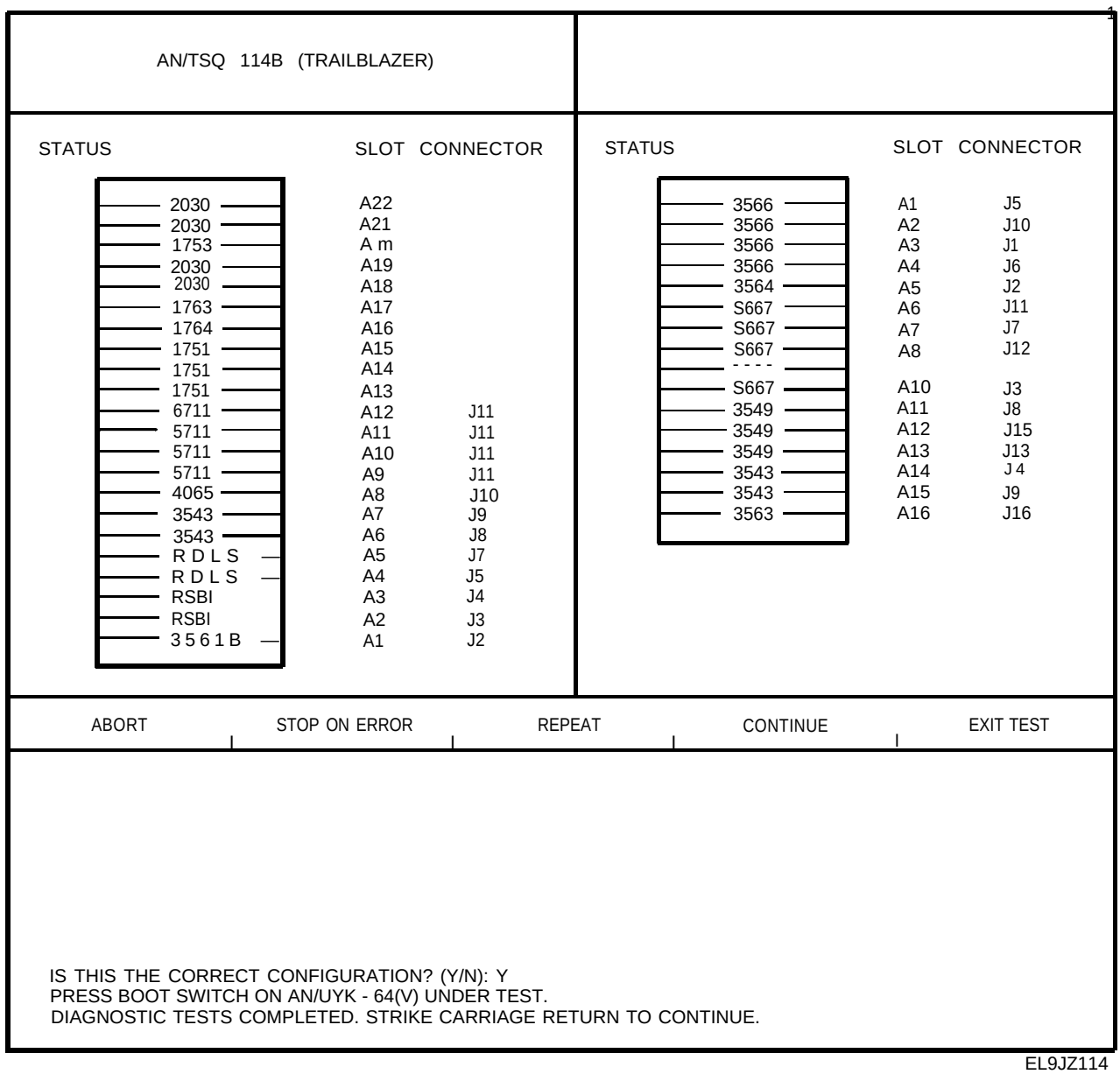

Figure 3-8. **Maintenance Diagnostic Display (Sheet 7 of 8)**

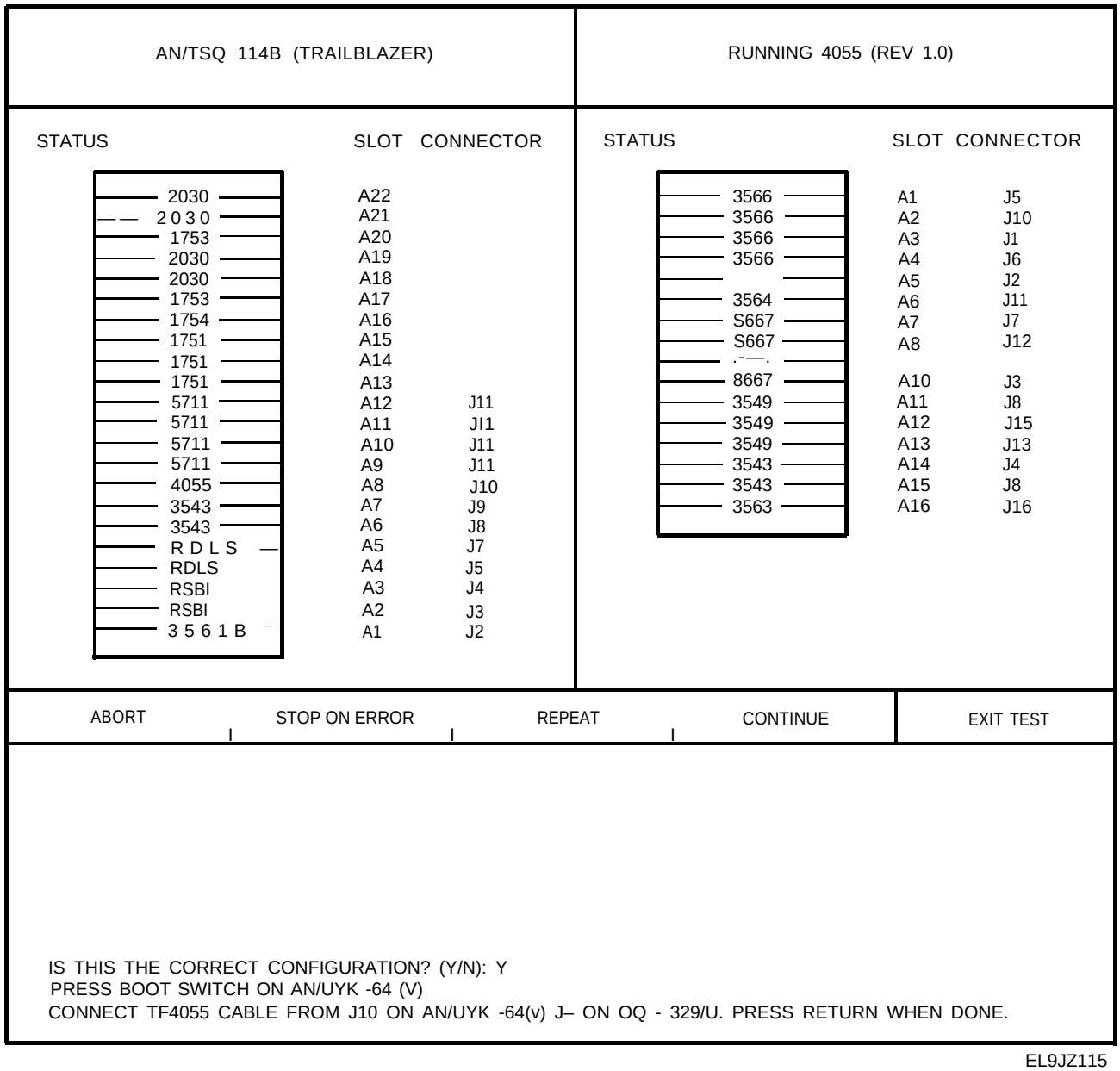

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Figure 3-8. Maintenance Diagnostic Display (Sheet 8 of 8)

Section IV. TESTING PROCEDURES

3-11. INTRODUCTION

This section provides procedures for testing the processor and those processor components that are serviceable at direct support maintenance. Differences between the core- and semiconductor-based processors, as applicable to testing, are noted in the testing procedures to follow.

3-12. PROCESSOR TESTING

This procedure is for setting up test equipment and the semiconductor or core memory processor in a testing configuration.

NOTE

Refer to the Maintenance Allocation Chart (MAC) in TM 11-7021-202-12 for definition of test equipment used in this testing configuration.

a. Diagnostic Setup

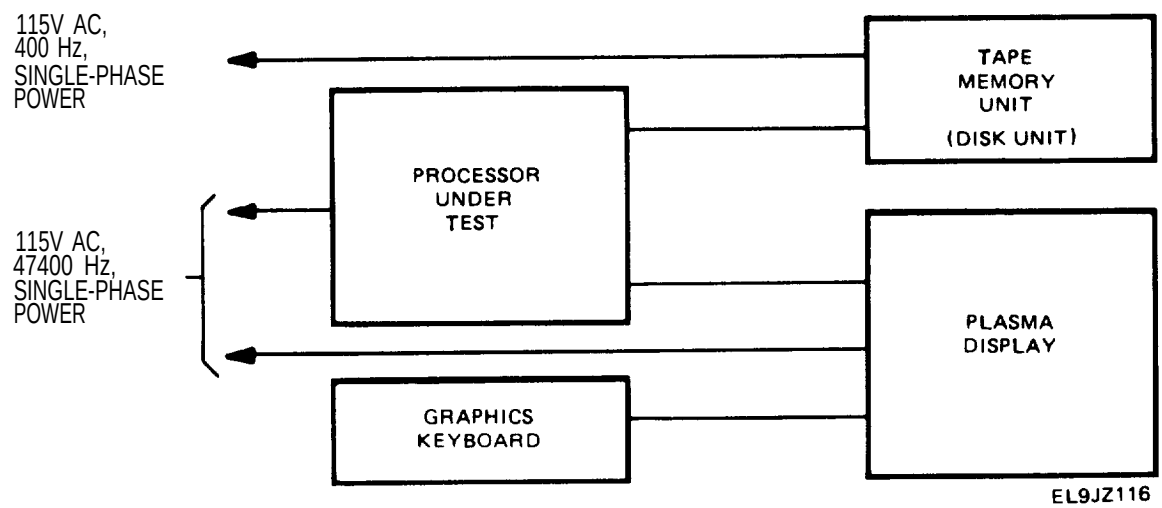
(1) Connect disk unit to processor under test with an I/O cable.

(2) Connect plasma display to processor under test with an I/O cable.

(3) Connect graphics keyboard to plasma display with keyboard cable.

(4) Connect tape memory unit to a source of 115 V ac, 400 Hz, single-phase power.

(5) Connect processor under test, and plasma display to a source of l15 V ac, 400 Hz, single-phase power.



b. Processor Setup.

(1) Remove top cover (para 3-27).

(2) Remove any circuit cards that are no tin the test configuration (para 3-29).

(3) install correct circuit cards in slots in processor (para 3-29).

(4) lf necessary, remove EMl filter (para 3-35) and power supply (para 3-34) and install correct EM I filter (para 3-35) and power supply (para 3-34).

(5) Install top cover (para 3-27).

(6) Run the diagnostic.

3-13. PRINTED CIRCUIT BOARD (PCB) TESTING

PCBs are tested with the processor (para 3-12). Detailed testing of PCBs is done at the next higher level of maintenance.

3-14. AC POWER SUPPLY OUTPUT VOLTAGES TEST

This procedure is for the semiconductor and core memory processors.

NOTE

Power supply output voltages are measured on the processor motherboard.

a. Remove bottom cover plate (para 3-28a)

WARNING

HIGH VOLTAGE is used in this equipment. **DEATH ON CONTACT** may result if safety precautions are not observed.

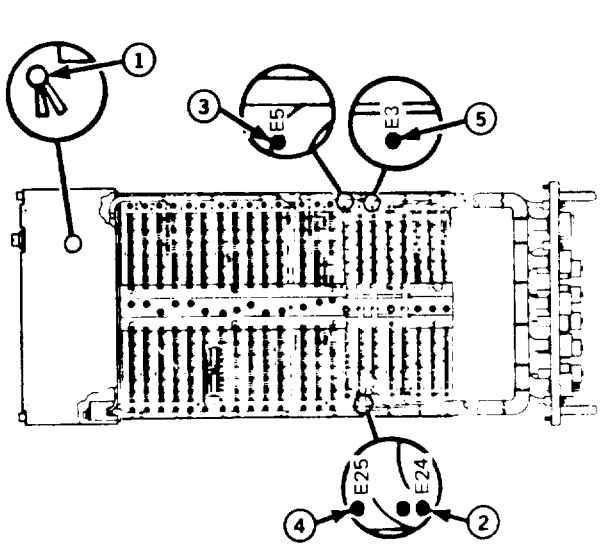
b. Apply power to processor. (TM 11-7021-202-12)

CAUTION

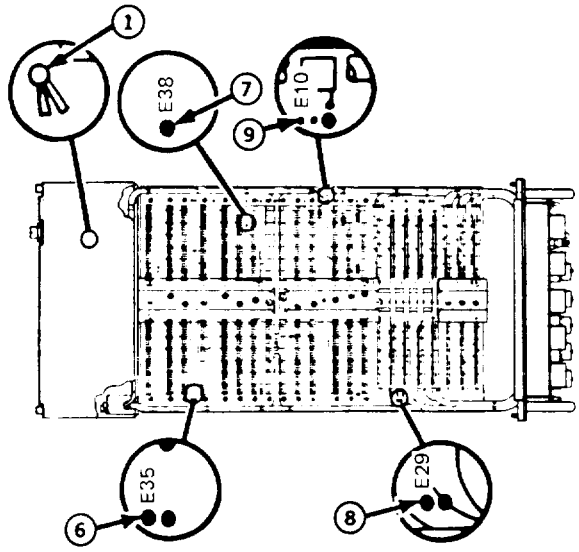
Care must be taken when using test probe. Failure to do so can cause shorts in equipment.

c. Connect the common (-) lead of a multimeter to a board ground (1).

d. Using the multimeter positive lead, measure power supply output voltages as shown in table 3-6.



SEMICONDUCTOR PROCESSOR



CORE MEMORY PROCESSOR

Table 3-6. Power Supply Output Voltages

Motherboard Test Point		
Semiconductor	**Core**	**Voltage**
E24 (2)	E35 (6)	+11.5 thru +12.5 V dc
E5 (3)	E38 (7)	-4.5 thru -5.5 V dc
E25 (4)	E29 (8)	-11.5 thru -12.5 V dc
E3 (5)	E1O (9)	+4.5 thru +5.5 V dc

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e. Remove power from processor (TM 11-7021-202-12

f. Install bottom cover plate (para 3-28).

3-15. DC POWER SUPPLY OUTPUT VOLTAGES TEST

The procedure for testing the dc power supply output voltages is the same as testing the ac power supply (para 3-14).

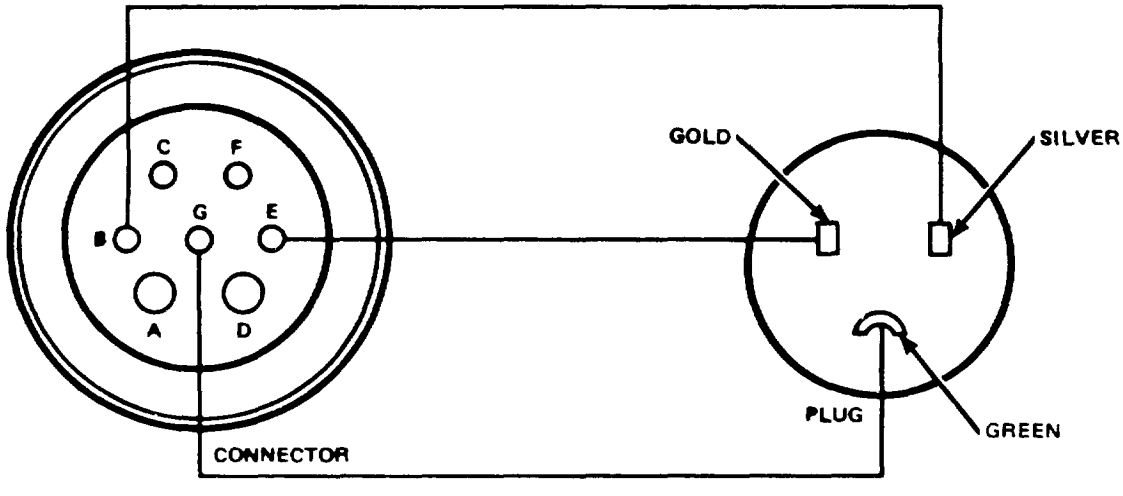
3-16. POWER CABLE CONTINUITY TEST

This procedure is for the semiconductor and core memory processors.

a. 220 V ac, 60 Hz, 1 PH Power Cable .

(1) Remove power cable (para 3-48a).

(2) Using a multimeter, check for continuity as indicated between the power cable plug and connector.



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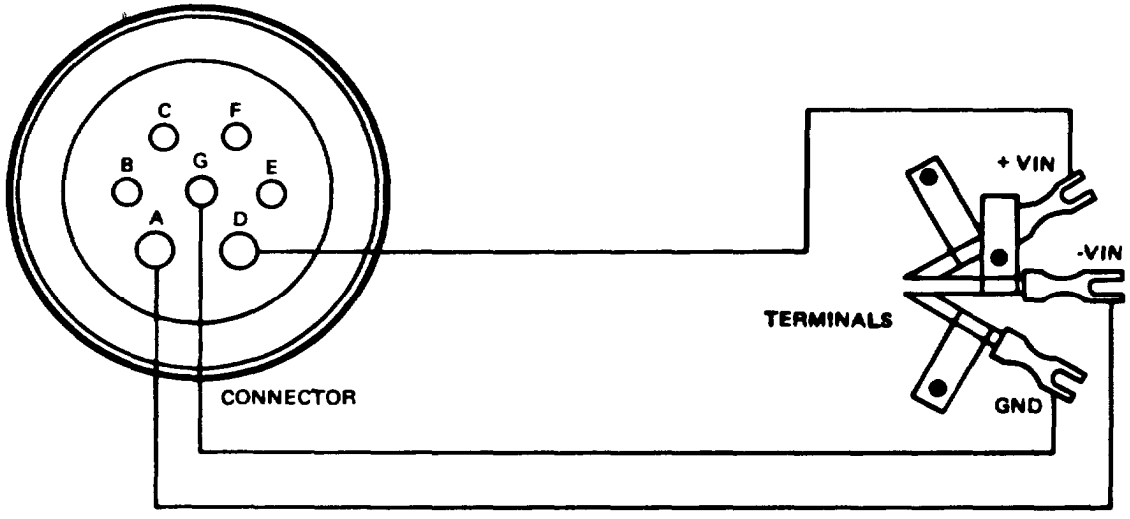
(3) install power cable (para 3-48d).

b. 24-28 V dc Power Cable.

(1) Remove power cable (para 3-48a).

(2) Using a multimeter, check for continuity between the power cable connector and terminals at points shown on diagram.



(3) Install power cable (para 3-48d).

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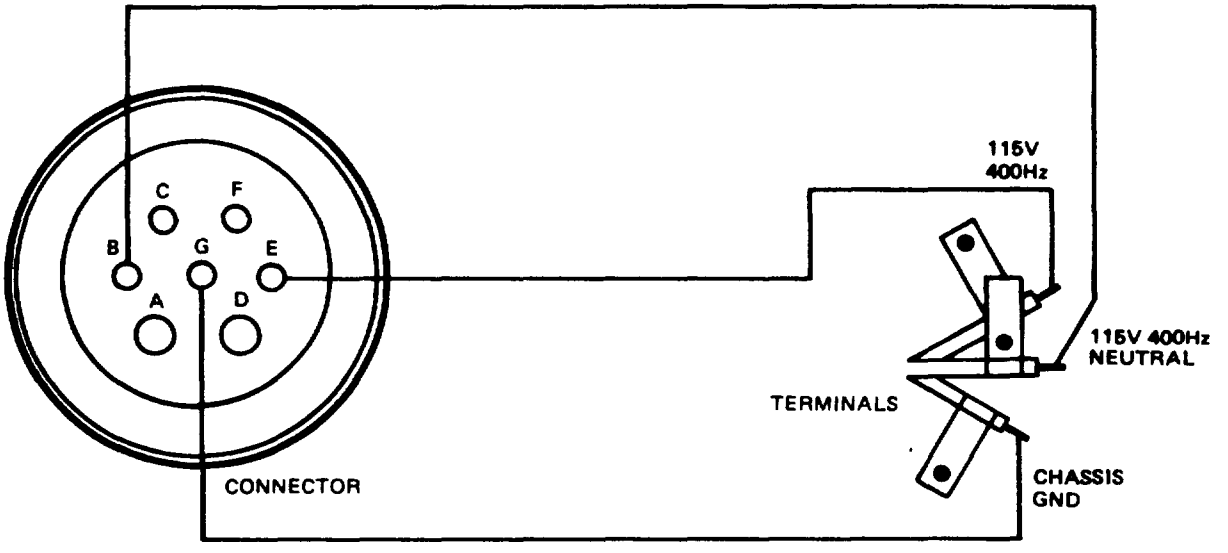
c. 115 V ac, 400 Hz, 1 PH Power Cable.

(1) Remove power cable (para 3-48a).

(2) Using a multimeter, check for continuity between the power cable connector and terminals at points shown on diagram.



(3) Install power cable (para 348d).

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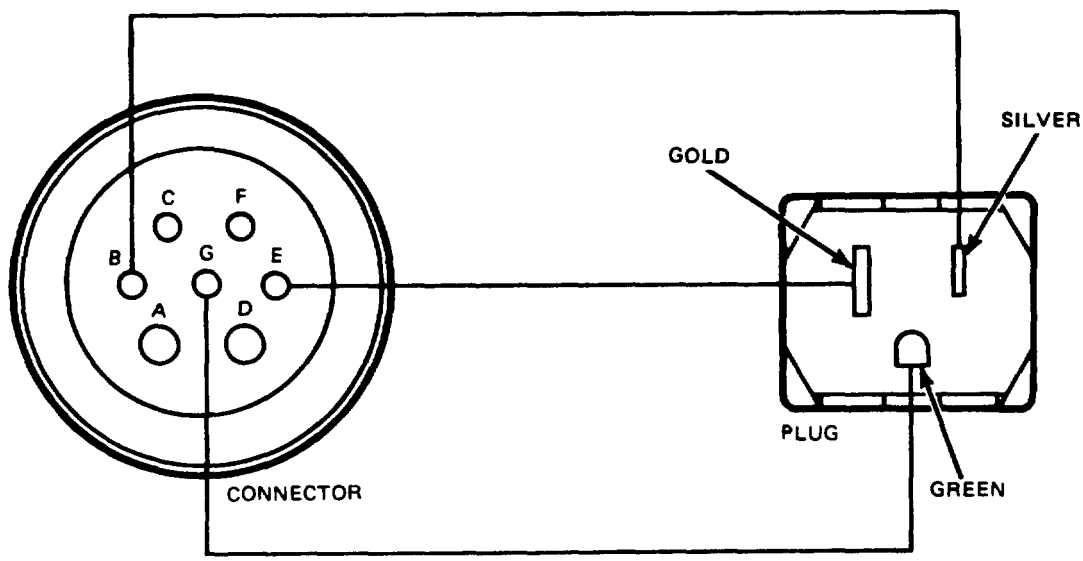
d. 115V ac, 60 Hz, 1 Power Cable.

(1) Remove power cable (para 3-48a).

(2) Using a multimeter, check the continuity between the power cable plug and connector.



(3) Install power cable (para 3-48d).

3-17. I/O CABLE CONTINUITY TEST

This procedure is for all cables connecting the 1/0 chassis to the semiconductor or core memory processor.

a. Remove I/O cable (para 3-47a).

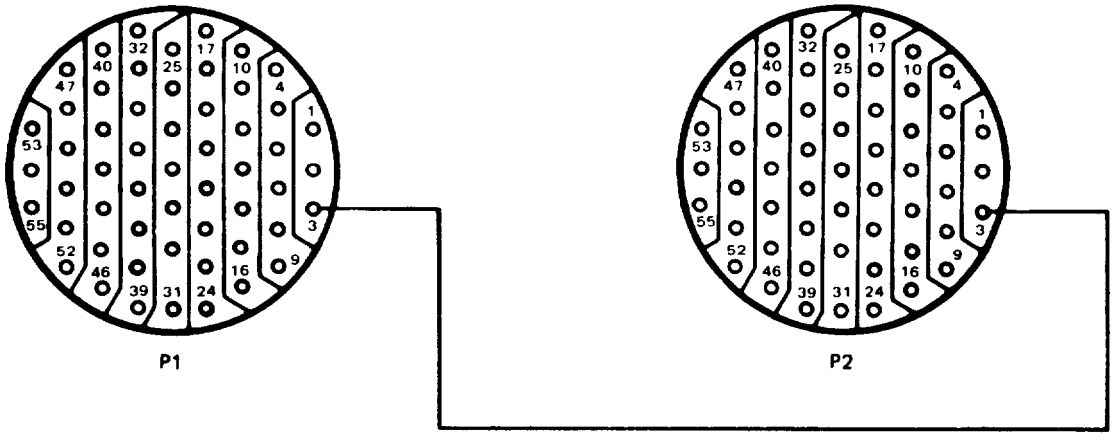
NOTE

Use a spare connector pin as an aid when performing cable continuity test.

EL9JZ121

b. Using a multimeter, check for continuity between pins 1 thru 55 on connector PI and the matching pin number on connector P2. Check between pin 1 on connector PI and pin 1 on connector P2.

c. Install I/O cable (para 3-47c).



3-18. PWR ON/RESET SWITCH TEST

This procedure is for the semiconductor and core memory processors.

WARNING

Turn off power before working on equipment. Failure to do so can cause serious injury to personnel.

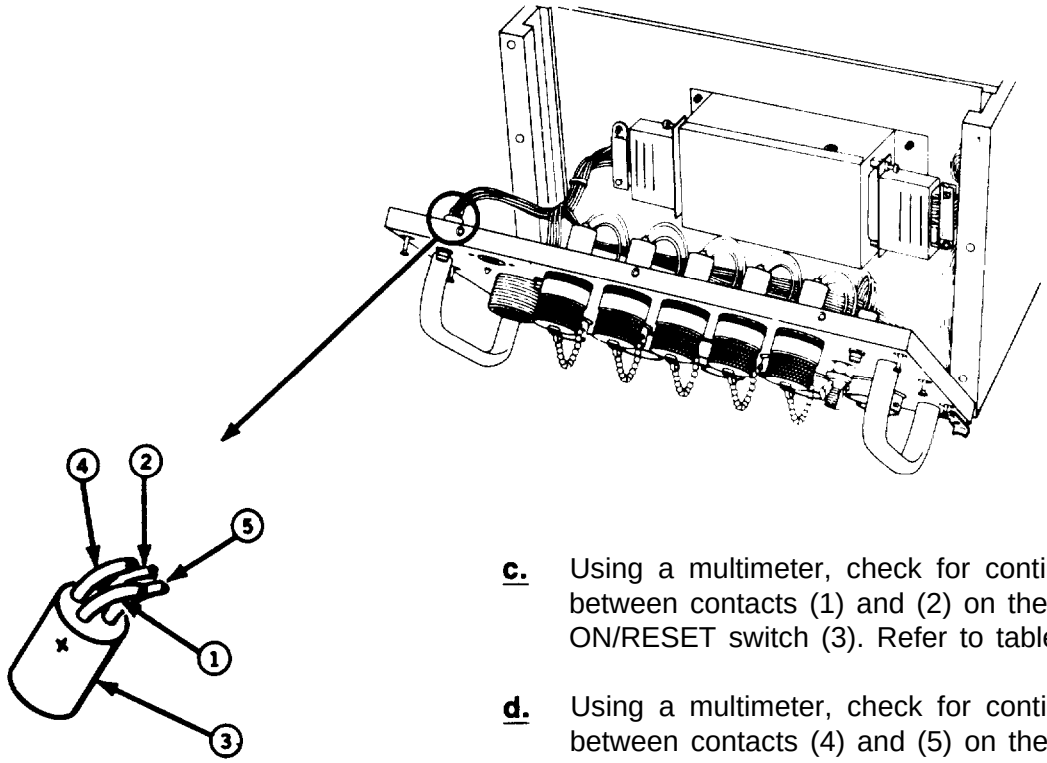
a. Remove (access) front panel (para 3-30).

b. Remove power supply (para 3-34).

NOTE

If one or both of the test probes are touching the PWR ON/RESET switch case while the continuity checks are being done, false readings may be obtained. Use needle probe to penetrate heat shrinkable tubing and touch contacts.

EL9JZ122



c. Using a multimeter, check for continuity between contacts (1) and (2) on the PWR ON/RESET switch (3). Refer to table 3-7.

d. Using a multimeter, check for continuity between contacts (4) and (5) on the PWR ON/RESET switch (3). Refer to table 3-7.

Table 3-7. PWR ON/RESET Switch Continuity

Measurement Between Pins (Callouts)	Switch not Depressed	Switch Depressed
1(+) and 2(-)	Continuity	Continuity
4(+) and 5(-)	No Continuity	Continuity

e. Install power supply (para 3-34).

WARNING

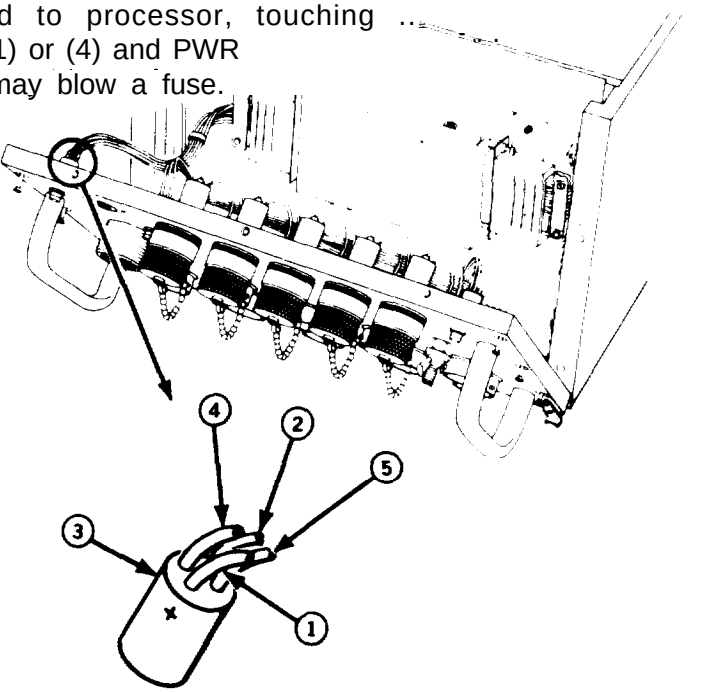
HIGH VOLTAGE is used in this equipment. **DEATH ON CONTACT** may result if safety precautions are not observed.

f. Apply power to processor (TM 11-7021-202-12).

EL9JZ123

CAUTION

When power is applied to processor, touching a test probe to contacts (1) or (4) and PWR ON/RESET switch case may blow a fuse.



g. Using a multimeter, check the voltage between contacts (1) and (2) on the PWR ON/RESET switch (3) (table 3-8).

h. Using a multimeter, check the voltage between contacts (4) and (5) on the PWR ON/RESET switch (3) (table 3-8).

Table 3-8. PWR ON/RESET Switch Voltages

Measurement Between Pins (Callouts)	Voltage	
	Switch not Depressed	Switch Depressed
1(+) and 2(-)	+4.5 thru + 5.5 V dc	0.0 V dc
4(+) and 5(-)	+ 27.5 thru +28.5 V dc	0.0 V dc

i. Remove power from processor (TM 11-7021-202-12).

j. Install front panel (para 3-30).

3-19. ELAPSED TIME METER (ETM) TEST

This procedure is for the semiconductor and core memory processors.

WARNING

Turn off power before working on equipment. Failure to do so can cause serious injury to personnel.

EL9JZ124

a. Remove (access) front panel (para 3-30).

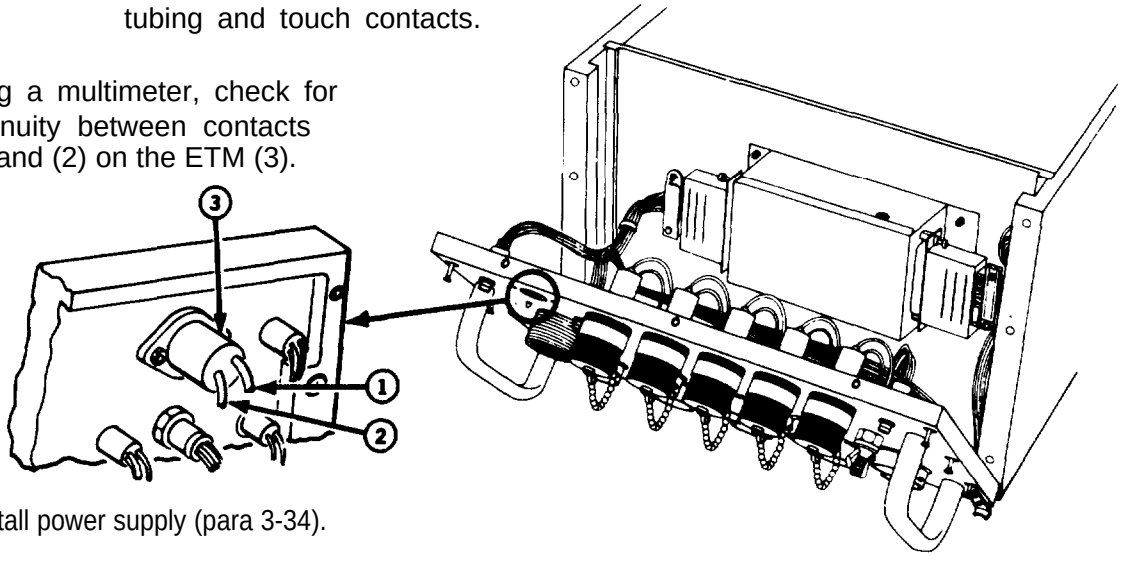
b. Remove power supply (para 3- 34).

NOTE

If one or both of the test probes are touching the ETM case while the continuity checks are being done, false readings may be obtained.

Use needle probe to penetrate heat shrinkable tubing and touch contacts.

c. Using a multimeter, check for continuity between contacts (1) and (2) on the ETM (3).



d. Install power supply (para 3-34).

e. Install front panel (para 3-30).

3-20. BITE/BOOT SWITCH TEST

This procedure is for the semiconductor and core memory processors

WARNING

Turn off power before working on equipment. Failure to do so can cause serious injury to personnel.

a. Remove front panel (para 3-30).

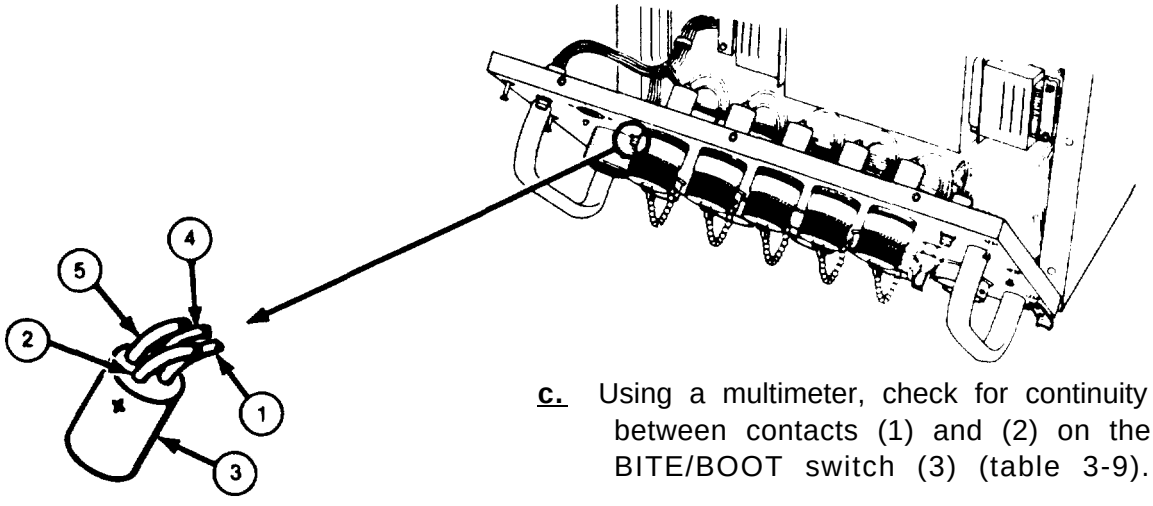
b. Remove power supply (para 3-34).

EL9JZ126

NOTE

If one or both of the test probes are touching the BITE/BOOT switch case while checking continuity, false readings may be obtained.

Use needle probe to penetrate heat shrinkable tubing and touch contacts.



c. Using a multimeter, check for continuity between contacts (1) and (2) on the BITE/BOOT switch (3) (table 3-9).

d. Using a multimeter, check for continuity between contacts (4) and (5) on the BITE/BOOT switch (3) (table 3-9).

Table 3-9. BITE/BOOT Switch Continuity

Measurement Between Pins (Callouts)	Continuity	
	Switch not Depressed	Switch Depressed
1(-) and 2(+)	Continuity	Continuity
4(-) and 5(+)	No Continuity	Continuity

e. Install power supply (para 3-34).

WARNiNG

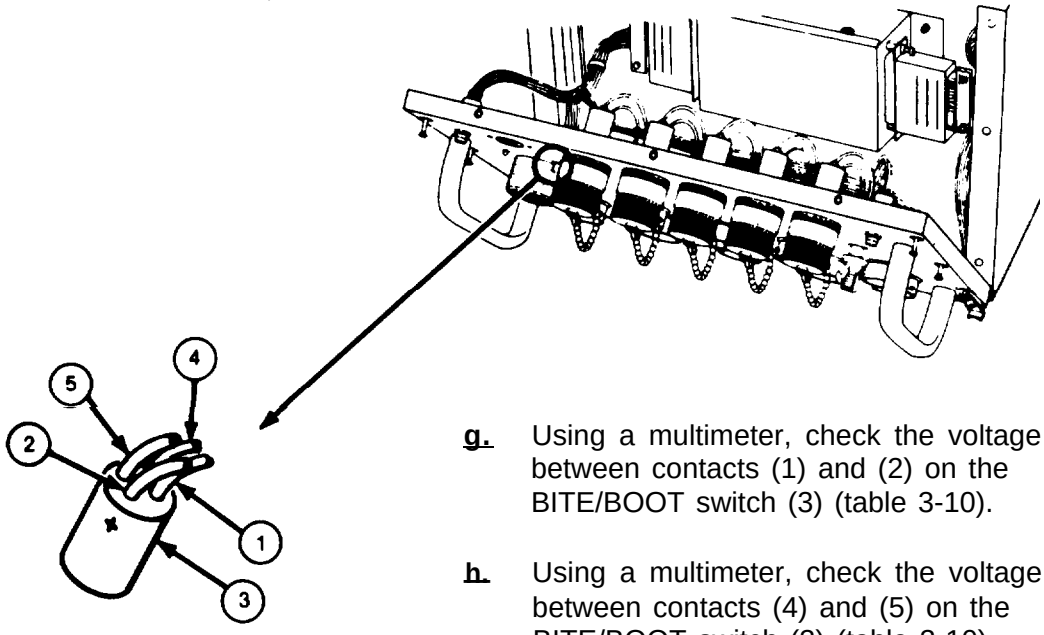
HIGH VOLTAGE is used in this equipment. **DEATH ON CONTACT** may result if safety precautions are not observed.

f Apply power to processor (TM 11-7021-202-12).

EL9JZ126

CAUTION

When power is applied to processor, touching a test probe to contacts (2) or (5) and switch case may blow a fuse.



g. Using a multimeter, check the voltage between contacts (1) and (2) on the BITE/BOOT switch (3) (table 3-10).

h. Using a multimeter, check the voltage between contacts (4) and (5) on the BITE/BOOT switch (3) (table 3-10).

Table 3-10. BITE/BOOT Switch Voltages

Measurement Between Pins (Callouts)	Voltage	
	Switch not Depressed	Switch Depressed
1(-) and 2(+)	+4.5 thru +5.5 V dc	0.0 V de
4(-) and 5(+)	+27.5 thru +28.5 V dc	0.0 V de

i. Remove power from processor (TM 11-7021-202-12).

J. Install front panel (para 3-30).

EL9JZ127

3-21. RUN/RESET SWITCH TEST

This procedure is for the semiconductor and core memory processors.

WARNING

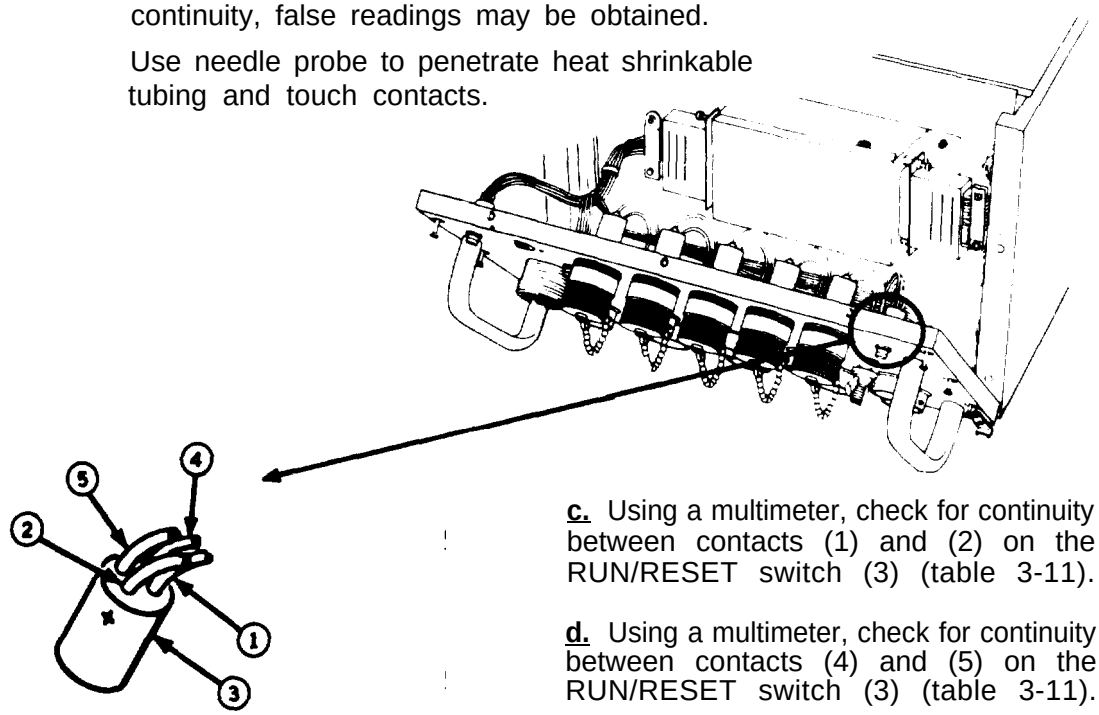
Turn off power before working on equipment. Failure to do so can cause serious injury to personnel.

a. Remove front panel (para 3-30).
b. Remove power supply (para 3-34).

NOTE

If one of the test probes are touching the RUN/RESET switch case while checking continuity, false readings may be obtained.

Use needle probe to penetrate heat shrinkable tubing and touch contacts.



c. Using a multimeter, check for continuity between contacts (1) and (2) on the RUN/RESET switch (3) (table 3-11).

d. Using a multimeter, check for continuity between contacts (4) and (5) on the RUN/RESET switch (3) (table 3-11).

Table 3-11. RUN/RESET Switch Continuity

Measurement Between Pins (Callouts)	Continuity	
	Switch not Depressed	Switch Depressed
1(-) and 2(+)	Continuity	Continuity
4(-) and 5(+)	No Continuity	Continuity

e. Install power supply (para 3-34).

WARNING

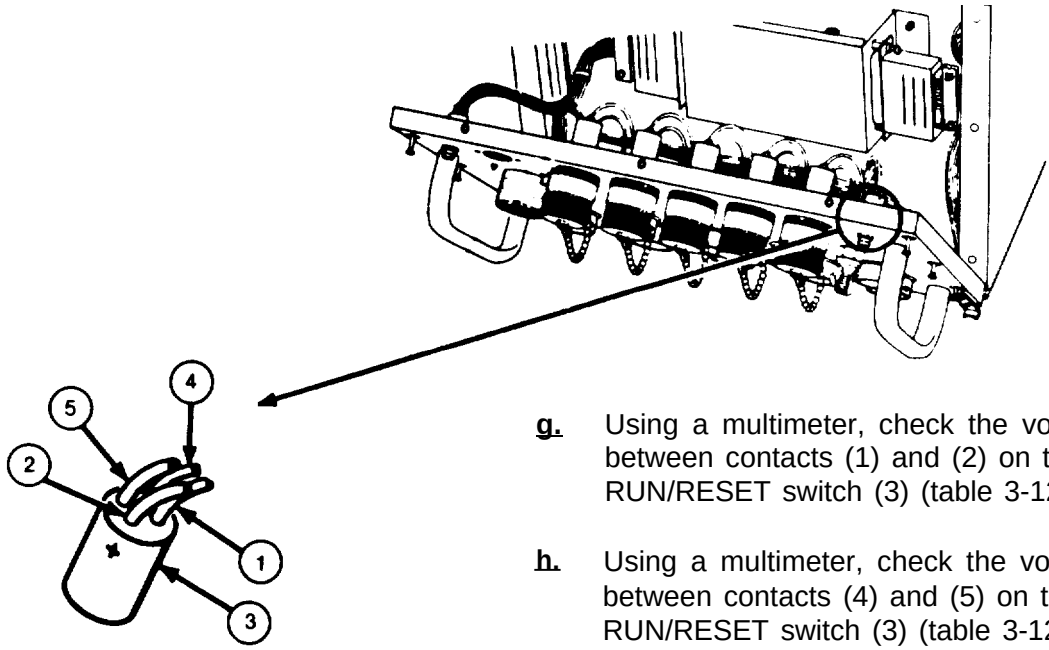
HIGH VOLTAGE is used in this equipment. **DEATH ON CONTACT** may result if safety precautions are not observed.

f. Apply power to processor (TM 11-7021-202-12).

EL9JZ128

CAUTION

When power is applied coprocessor, touching a test probe to contacts (2) or (5) and switch case may blow a fuse.



g. Using a multimeter, check the voltage between contacts (1) and (2) on the RUN/RESET switch (3) (table 3-12).

h. Using a multimeter, check the voltage between contacts (4) and (5) on the RUN/RESET switch (3) (table 3-12).

Table 3-12. RUN/RESET Switch Voltages

Measurement Between Pins (Callouts)	Voltage	
	Switch not Depressed	Switch Depressed
1(-) and 2(+)	+4.5 thru +5.5 V dc	0.0 V dc
4(-) and 5(+)	+27.5 thru +28.5 V dc	0.0 V dc

i. Remove power from processor (TM 11-7021-202-12).

j. Install front panel (para 3-30).

EL9JZ129

3-22. BATT INDICATOR TEST

This procedure is for the semiconductor processor only.

WARNING

Turn off power before working on equipment. Failure to do so can cause serious injury to personnel.

a. Remove front panel (para 3-30).

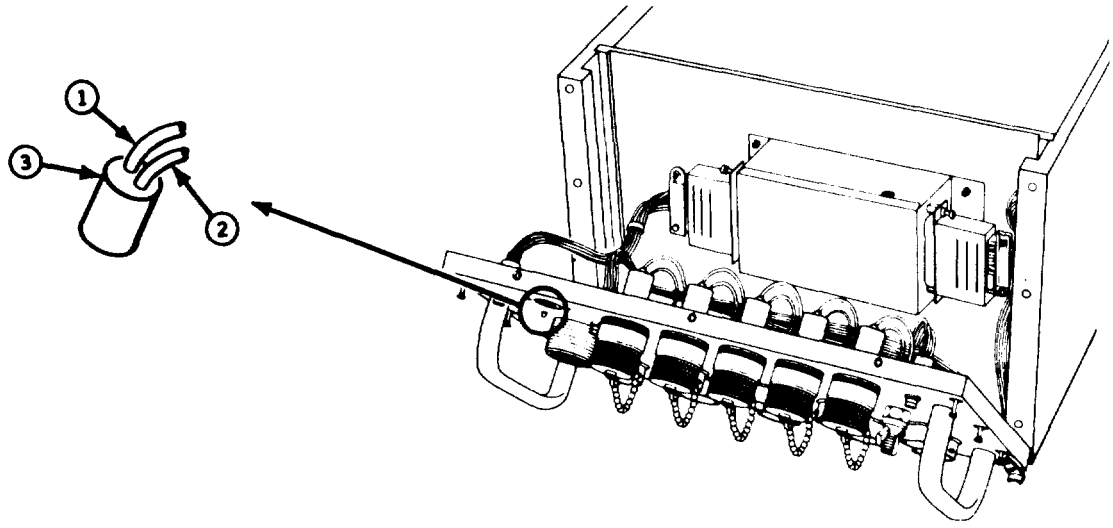
b. Remove power supply (para 3-34).

NOTE

If one or both of the test probes are touching the BAIT indicator case while checking continuity, false readings may be obtained.

Use needle probe to penetrate flat shrinkable tubing and touch contacts.

c. Using a multimeter, check for continuity between contacts (1) and (2) on the BATT indicator (3).



d. Install power supply (para 3-34).

EL9JZ130

WARNING

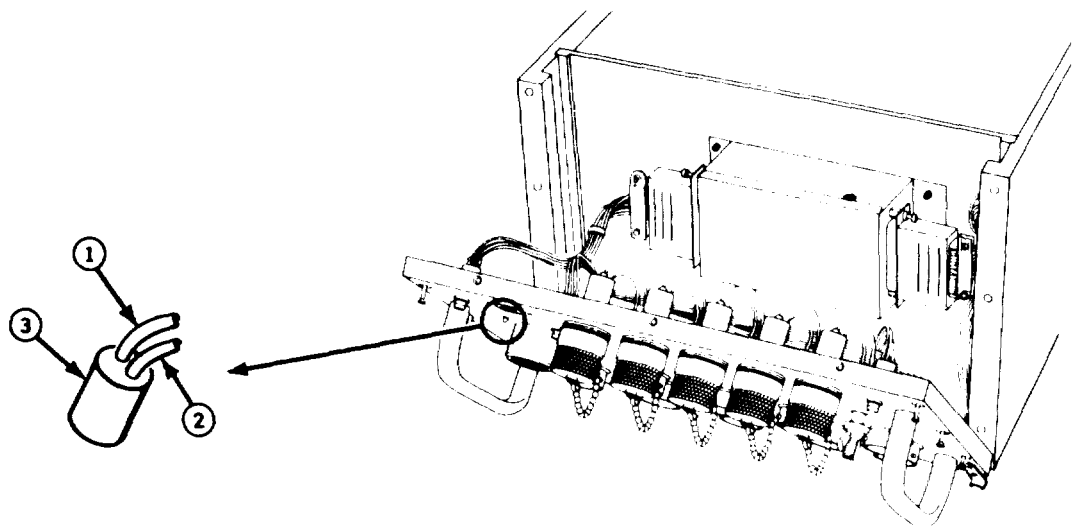
HIGH **VOLTAGE** is used in this equipment. **DEATH ON CONTACT** may result if safety precautions are not observed.

e. Apply power to processor (TM 11-7021-202-12).

CAUTION

When power is applied to processor, touching a test probe to contact (2) and switch case may blow a fuse.

f. Using a multimeter, check that 5 V dc is at contact (2) (red wire).



g. Remove power from processor (TM 11-7021-202-12).

h. Install front panel (para 3-30).

3-23. POWER UNIT ASSEMBLY (AC AND DC)

This procedure is for the semiconductor and core memory processors.

WARNING

Turn off power before working on equipment. Failure to do so can cause serious injury to personnel.

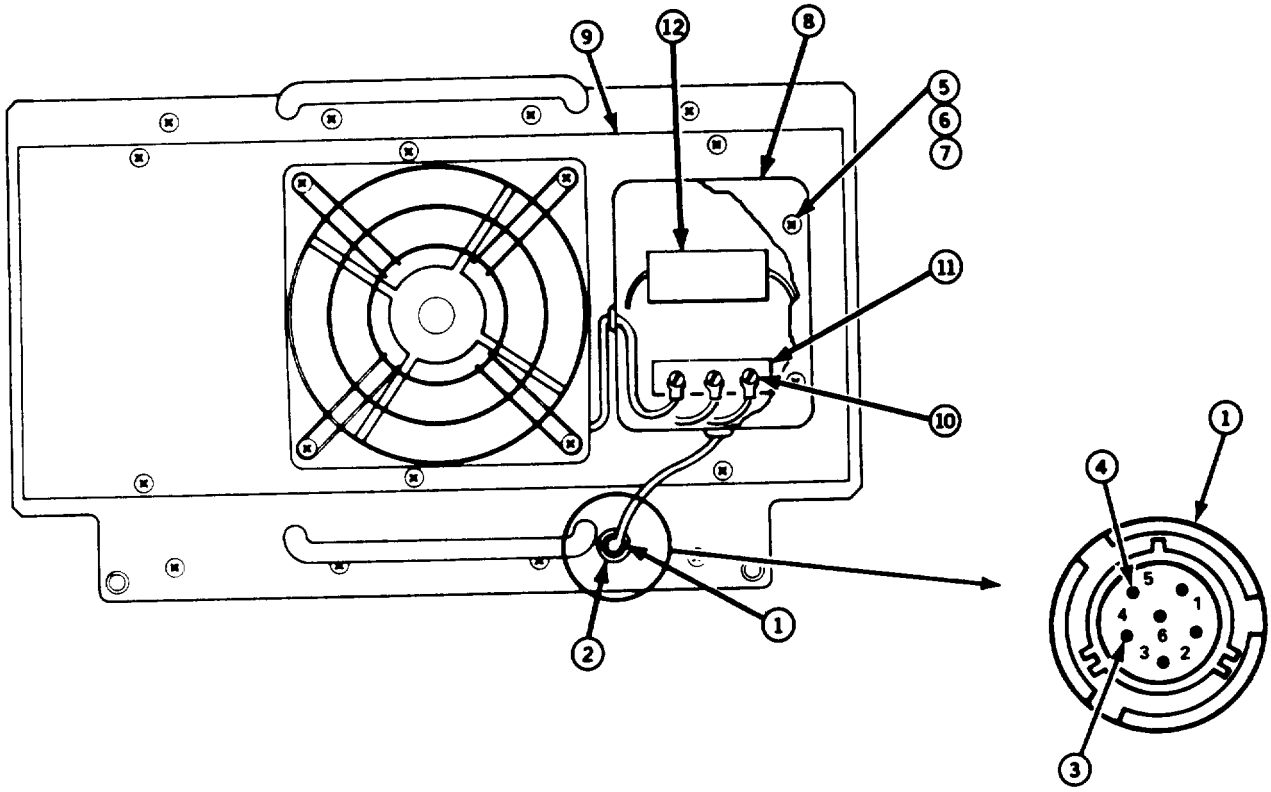
EL9JZ131

a. AC Power Unit Assembly.

(1) Disconnect plug P1 (1) from power supply connector J17 (2).

(2) Using a multimeter, check for continuity between pins 4 (3) and 5 (4) on plug P1 (1).

(3) Remove four screws (5), lock washers (6), and washers (7) from cover (8), and remove cover (8) from power unit (9).



(4) Using a multimeter, check for continuity between terminal TB1 -3 (10) on the power unit terminal board (11) and pin 5 (4) on plug P1 (1).

(5) Check capacitor C1 (12).

(6) Position cover (8) on power unit (9) and install four screws (5), washers (7), and lock washers (6).

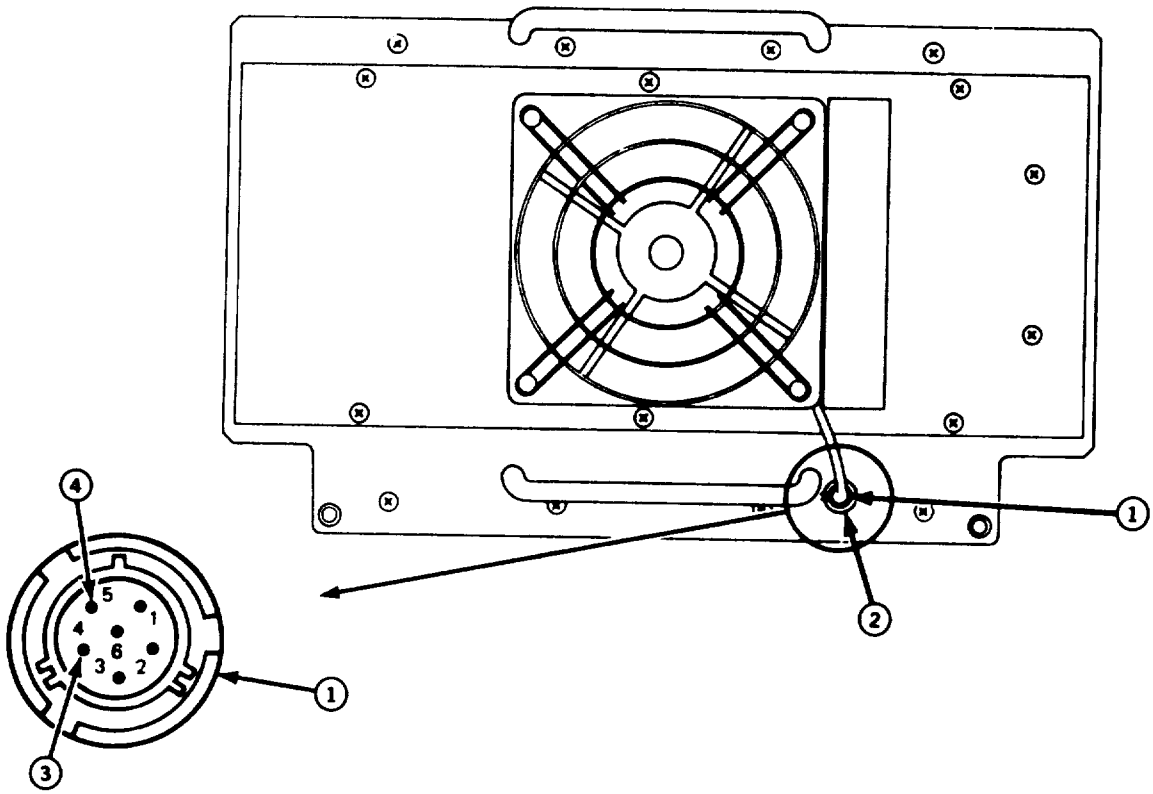
(7) Connect plug P1 (1) to power supply connector J17 (2).

EL9JZ132

b. DC Power Unit Assembly.

(1) Disconnect plug P1 (1) from power supply connector J17 (2).

(2) Using a multimeter, check for continuity between pins 4 (3) and 5 (4) on plug P1 (1).



(3) Connect plug P1 (1) to power supply connector J17 (2).

3-24. MOTHERBOARD TESTING

Motherboard testing consists of checking for continuity between connectors, using a multimeter. For voltage potential tests, refer to paragraph 3-14. Further testing of the motherboard is done at the next higher level of maintenance.

3-25. CHASSIS TESTING

Chassis testing consists of checking for chassis continuity and voltage potentials.

Using a multimeter, check for continuity and voltage potentials between chassis ground and various points on the chassis.

EL9JZ133

Section V. REMOVAL AND REPLACEMENT PROCEDURES

3-26. INTRODUCTION

This section provides procedures for removing and replacing processor components that are serviceable at direct support maintenance. Differences between the core- and semiconductor-based processors, as applicable to removal and replacement, are noted in the following procedures.

3-27. TOP FRONT COVER PLATE REMOVAL AND REPLACEMENT

This procedure is for the semiconductor and core memory processors.

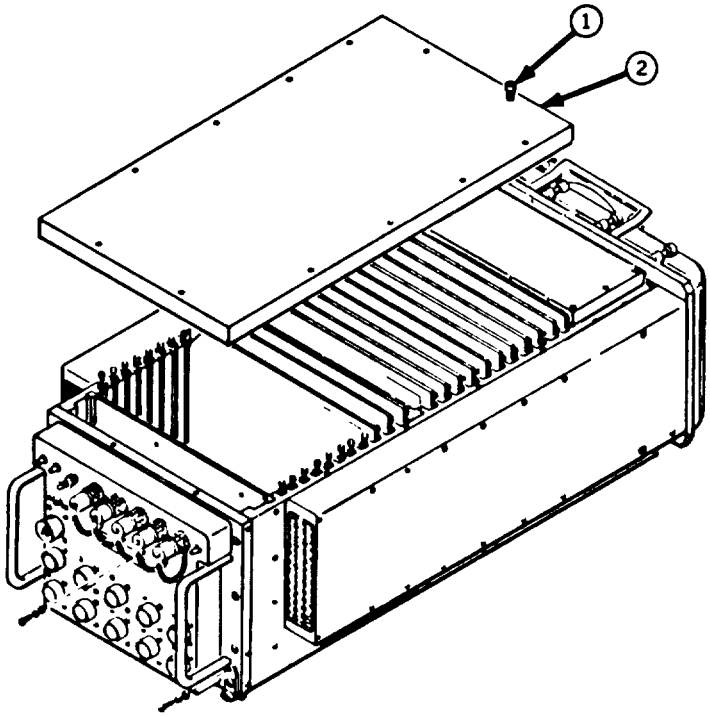
WARNING

Turn off power before working on equipment. Failure to do so can cause serious injury to personnel.

a. Removal.

(1) Loosen 16 captive screws (1) on top front cover plate (2).

(2) Remove top front cover plate (2).

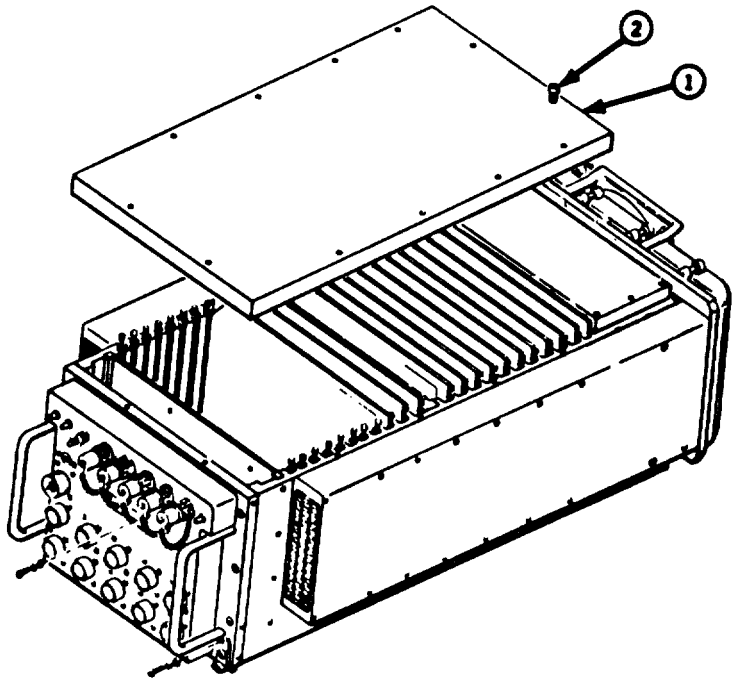


EL9JZ134

b. Replacement.

(1) Position top front cover plate (1) on processor.

(2) Tighten 16 captive screws (2).



3-28. BOTTOM COVER PLATE REMOVAL AND REPLACEMENT

This procedure is for the semiconductor and core memory processors.

WARNING

Turn off power before working on equipment. Failure to do so can cause serious injury to personnel.

The processor is a heavy piece of equipment. Always use three technicians when moving or lifting the unit to prevent personal injury.

NOTE

The processor must be on its side to perform this procedure.

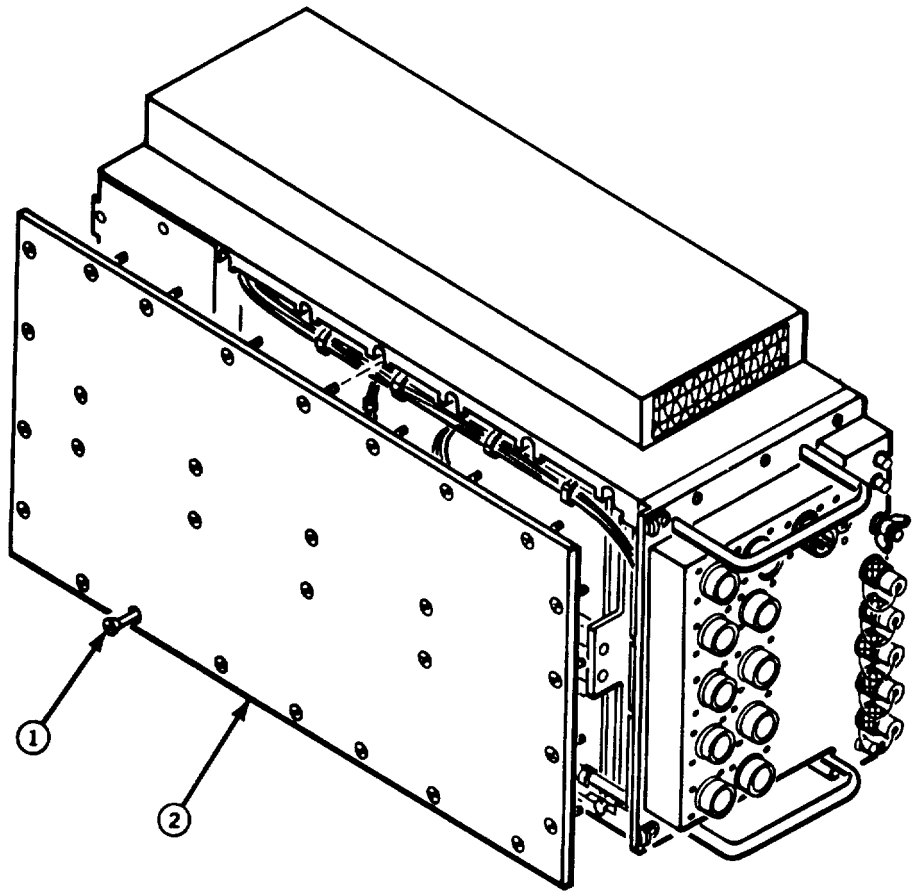
EISJZ136

a. Removal.

(1) Place processor on its side as shown in illustration.

(2) Loosen 28 captive screws (l) from bottom cover plate (2).

(3) Remove bottom cover plate.

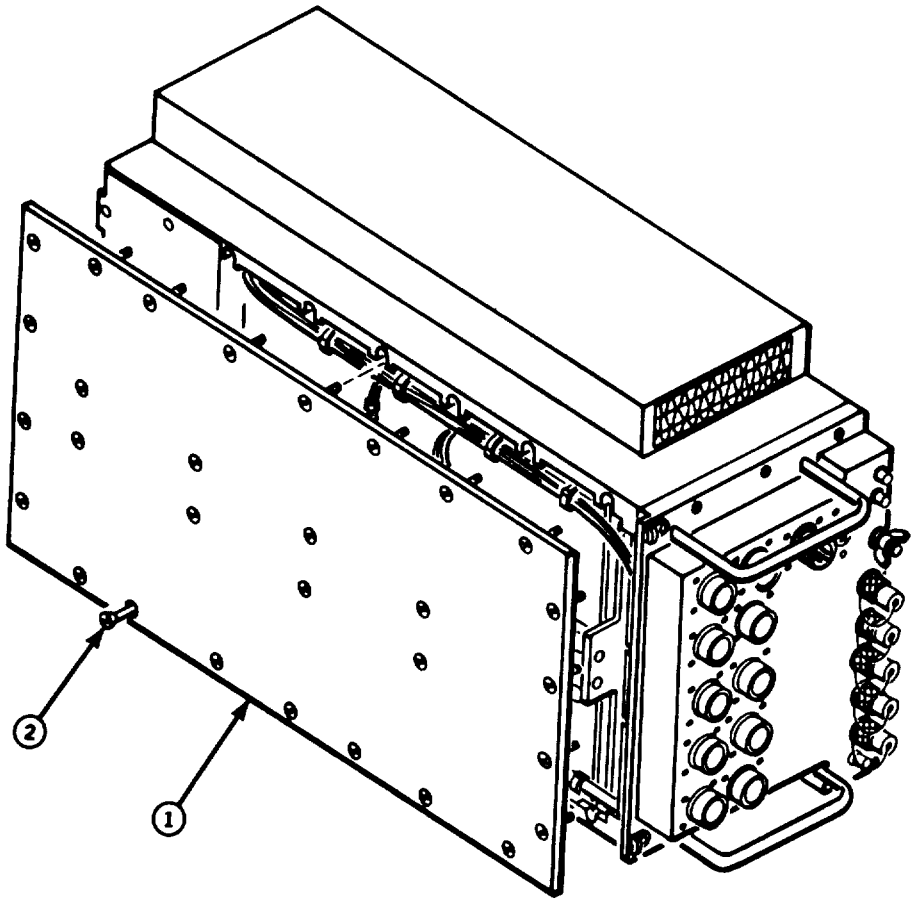


EL9JZ136

b. Replacement.

(1) Position bottom cover plate (1) on processor.

(2) Tighten 28 captive screws (2) in bottom cover plate (1).



3-29. PCB REMOVAL AND REPLACEMENT

This procedure is typical for all processor circuit boards on the semiconductor and core memory processors.

EL9JZ137

WARNING

Turn off power before working on equipment. Failure to do so can cause serious injury to personnel.

a. Removal.

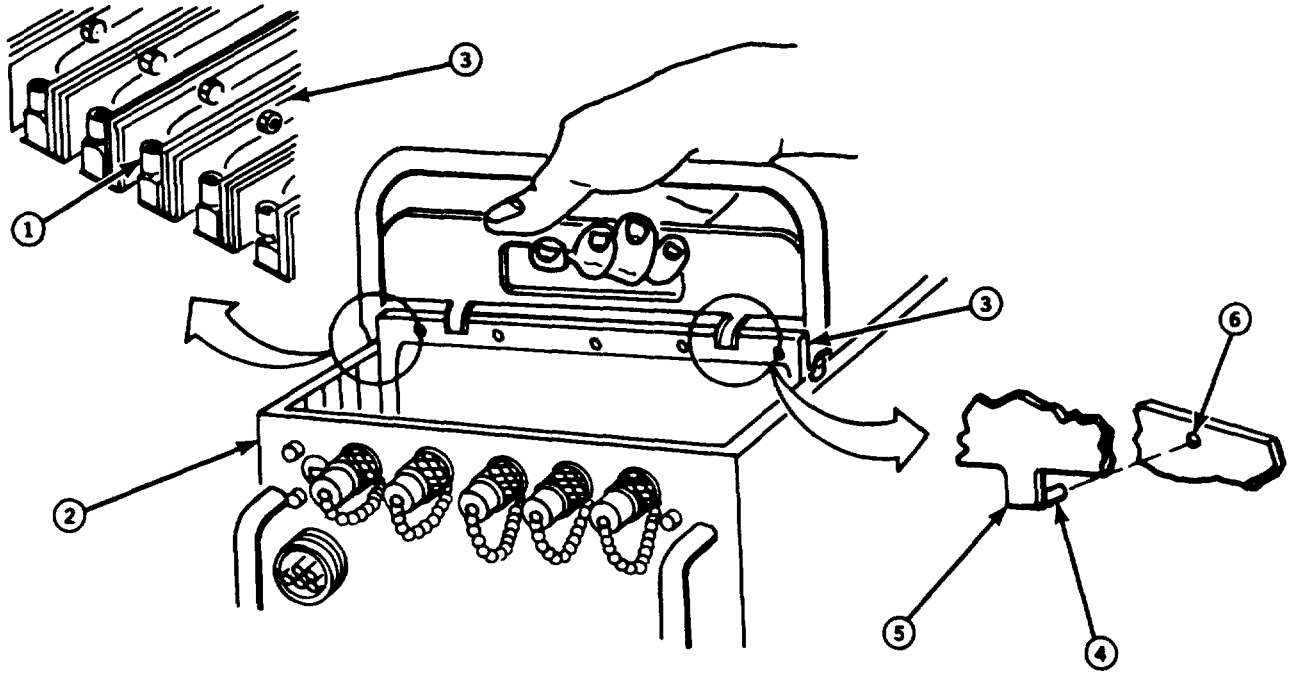
(1) Remove top front cover plate (para 3-27).

(2) Loosen two wedge screws (1) five or six turns, one on each side of processor (2), to release PCB board (3).

NOTE

Pins on extractor tool must be inserted from metal side of PCB holes.

(3) Aline two pins (4) on extractor tool (5) with holes (6) in PCB (3). Squeeze extractor tool handle to disconnect PCB. Remove it by pulling straight up.



EL9JZ138

b. Replacement.

CAUTION

Do not use force when installing PCBs. PCBs can be damaged if forced into place.

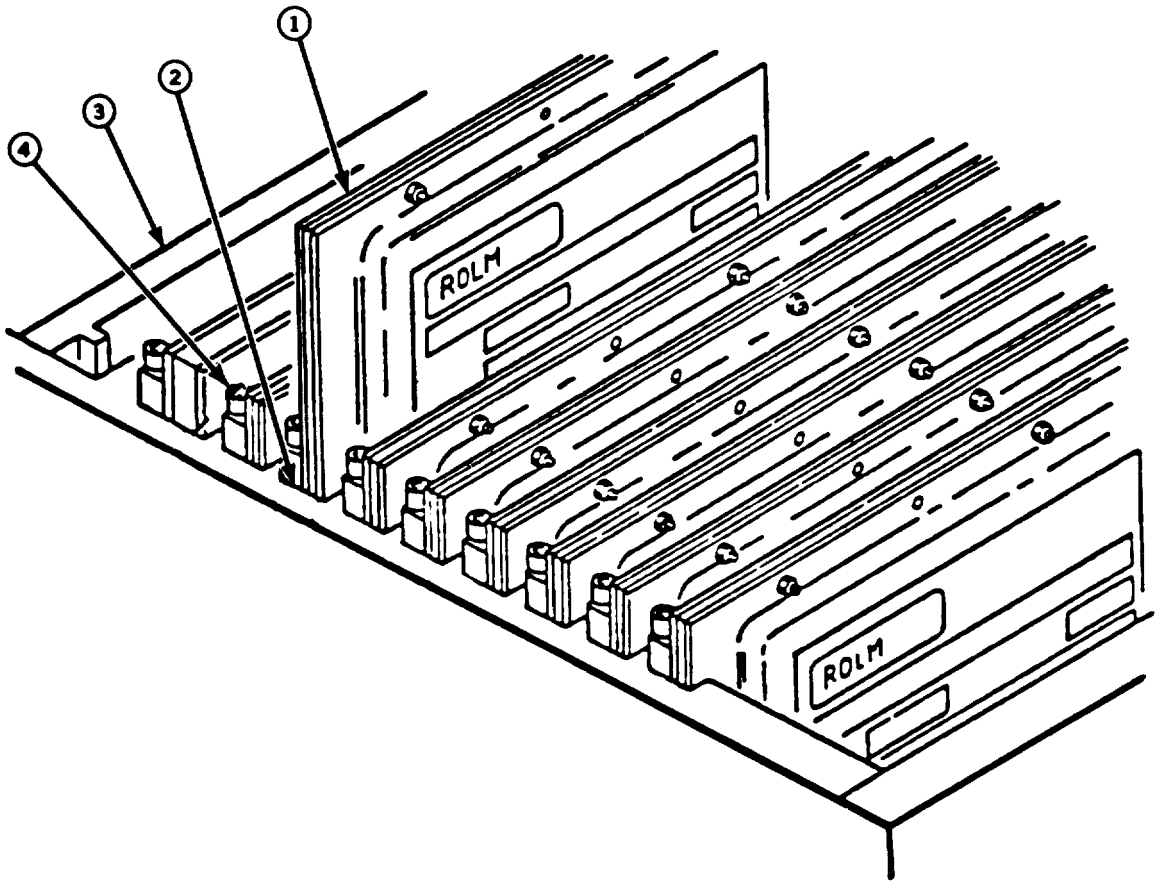
NOTE

Loosen or tighten wedge screws as required to install PCBs in slots.

(1) Aline circuit card (1) with slots (2) in processor (3) and carefully press PCB straight down. Make sure PCB is properly seated.

(2) Tighten two wedge screws (4), one on each side of processor (3), securing PCB (1).

(3) Install top front cover plate (para 3-27).



EL9JZ139

3-30 REMOVE (ACCESS) AND REPLACE (SECURE) FRONT PANEL

This procedure is for the semiconductor and core memory processors.

WARNING

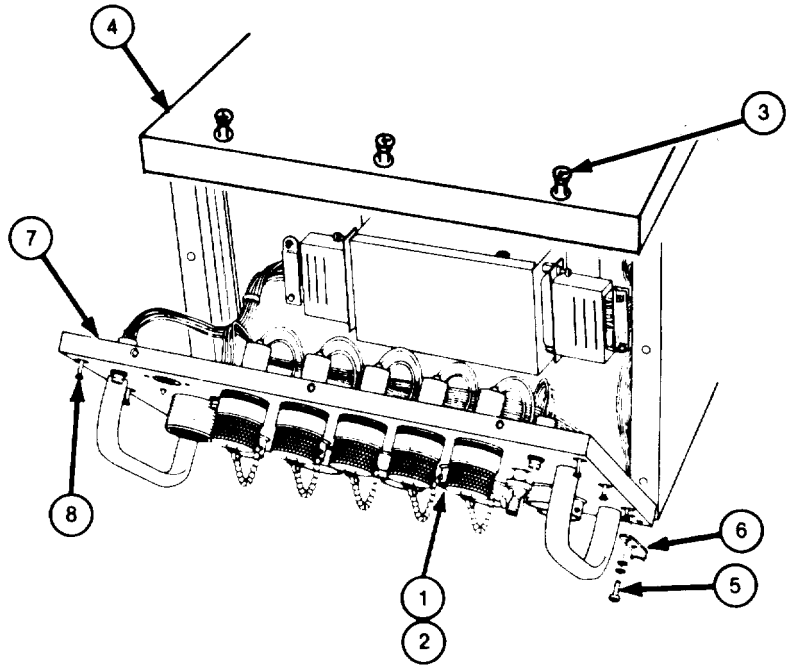
Turn off power before working on equipment. Failure to do so can cause serious injury to personnel.

a. Removal.

(1) Loosen two captive screws (located but not shown) (1) at front of bottom cover plate (2) until they pop up.

(2) Loosen three captive screws (3) on top cover plate (4) until they pop up.

(3) Remove four screws (5) and two hooks (6) from front panel (7).



CAUTION

Processor must be on flat surface. Do not tilt front panel more than needed to reach component.

(4) Loosen six captive screws (8) and tilt front panel (7) forward.

EL9JZ140

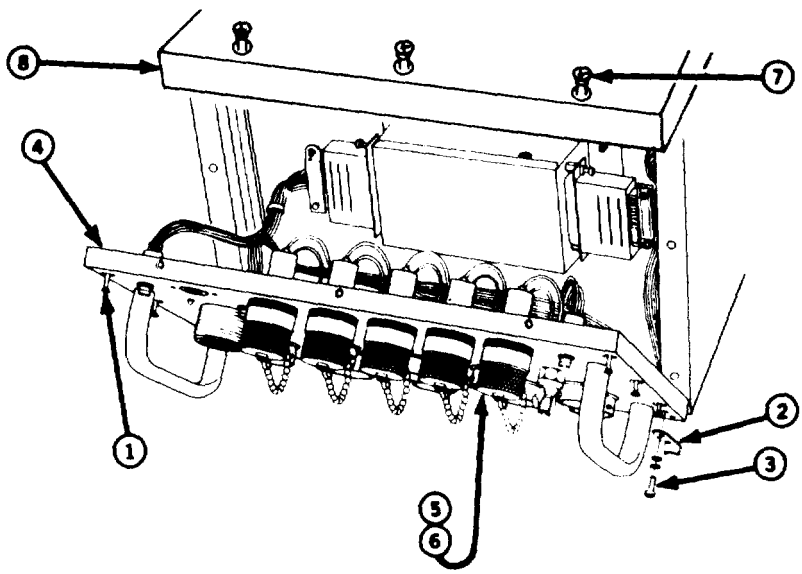
b. Replacement.

(1) Aline six captive screws (1) with holes in side covers. Tighten six captive screws (1).

(2) install two hooks (2) and four screws (3) on front panel (4).

(3) Tighten two captive screws (5) (located but not shown) at front of bottom cover plate (6).

(4) Tighten three captive screws (7) on top cover plate (8).



3-31. AIR DUCT REMOVAL AND REPLACEMENT

This procedure is for the semiconductor and core memory processors.

WARNING

Turn off power before working on equipment. Failure to do so can cause serious injury to personnel.

ELSJZ141

a. Removal.

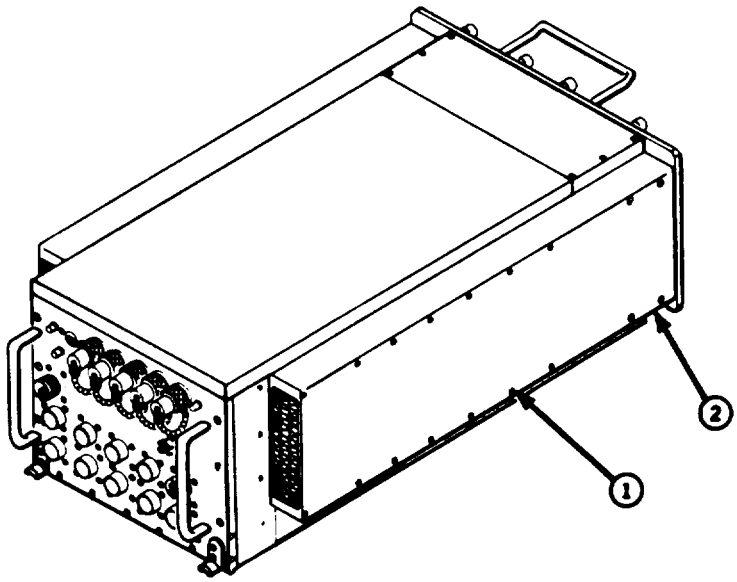
(1) Remove 18 screws (l) from air duct (2).

(2) Remove air duct (2).

b. Replacement.

(1) Add thermal paste (appx D, item 21) between air duct (2) and processor. Position heat air duct (2) on processor.

(2) Install and tighten 18 screws (1) on heat air duct.



ELWZ142

3-32. BLOWER FAN REMOVAL AND REPLACEMENT

This procedure is for the semiconductor and core memory processors. The differences between the ac and dc blower fans are shown in the illustrations and are noted in the procedure.

WARNING

Turn off power before working on equipment. Failure to do so can cause serious injury to personnel.

a. Removal.

(1) Remove plug (1) from power supply connector (2).

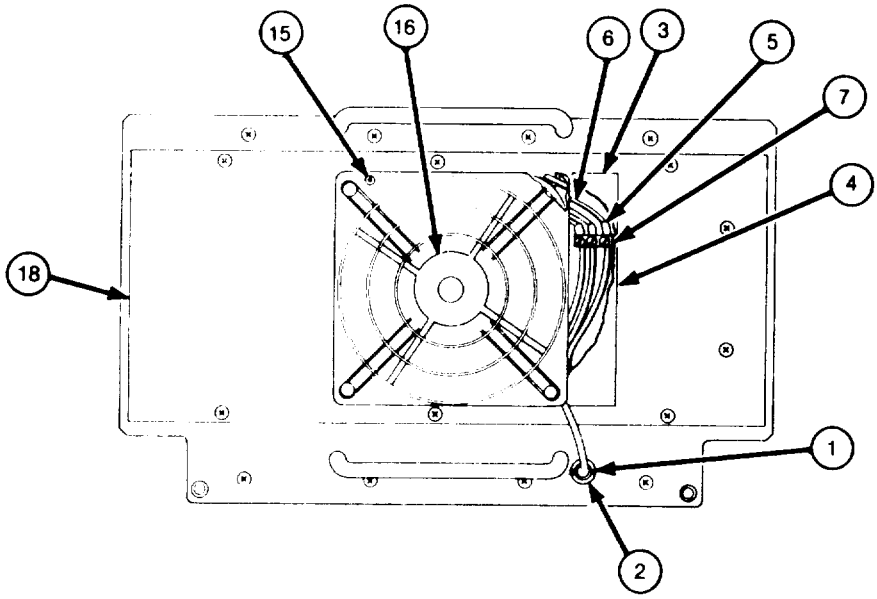
NOTE

Steps 2 thru 4 are for the dc blower fan only.

(2) Loosen four captive screws (3) and remove terminal box (4).

(3) Cut and remove heat shrinkable tubing (5) from three wires (6).

(4) Unsolder and remove three wires (6) from terminal strip (7).



EL9JZ143

NOTE

Steps 5 thru 8 are for the ac blower fan only.

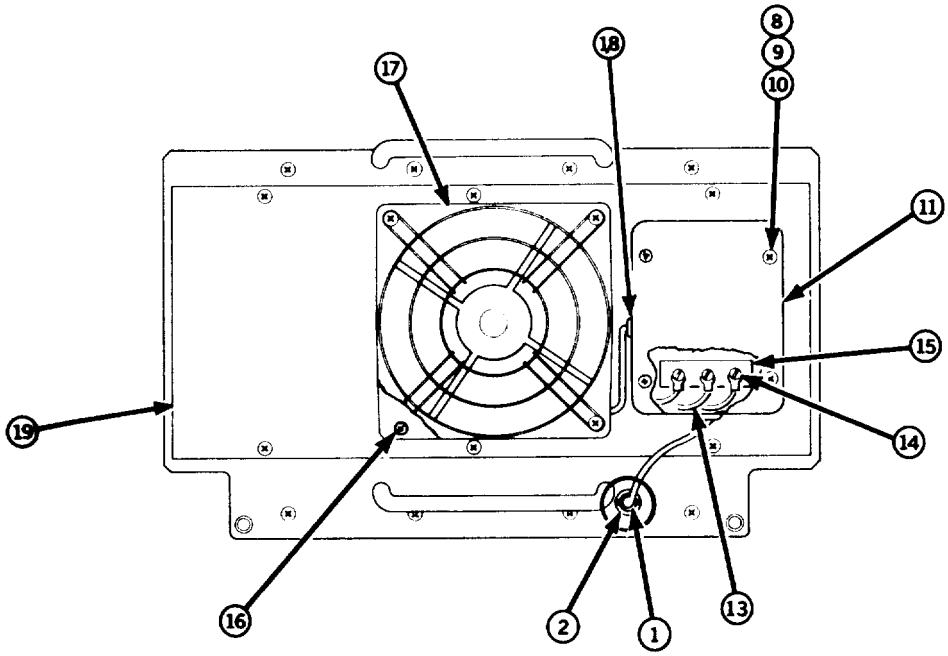
(5) Remove four screws (8), lockwashers (9), and flat washers (10). Remove terminal box cover (11).

(6) Loosen three terminal screws (14) and remove three wires (13) from terminals 1, 2, and 3 on terminal strip (15). Tag terminals.

(7) Remove four screws (16) from base of blower fan (17).

(8) Remove three wires (13) and rubber grommet (18) from terminal box (11).

(9) Remove blower fan (17) from power unit assembly (19).



AC BLOWER FAN

EL9JZ144

b. Replacement

(1) Position blower fan (1) on power unit assembly (2).

(2) Install four screws (3) on base of blower fan (1).

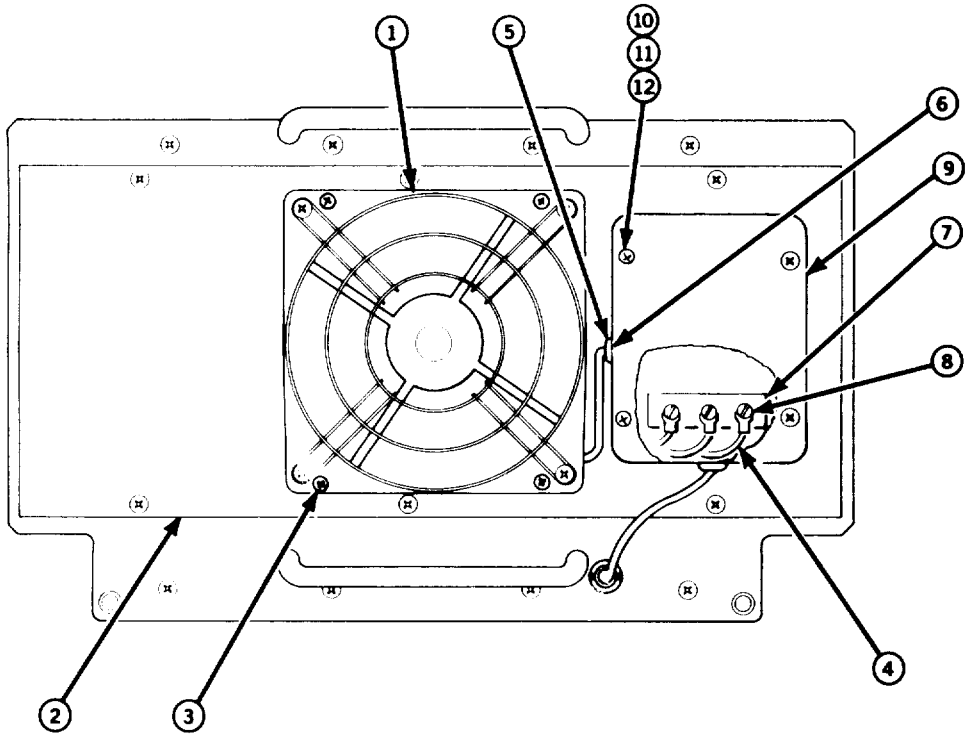
NOTE

Steps 3 thru 5 are for the ac blower fan only.

(3) Insert three wires (4) and rubber grommet (5) into hole (6) on side of terminal box.

(4) Install three wires (4 on terminal strip (7) and tighten three terminal screws (8).

(5) Position terminal box cover (9). install four flat washers (10), lock washers (11), and screws (12).



AC BLOWER FAN

EL9JZ145

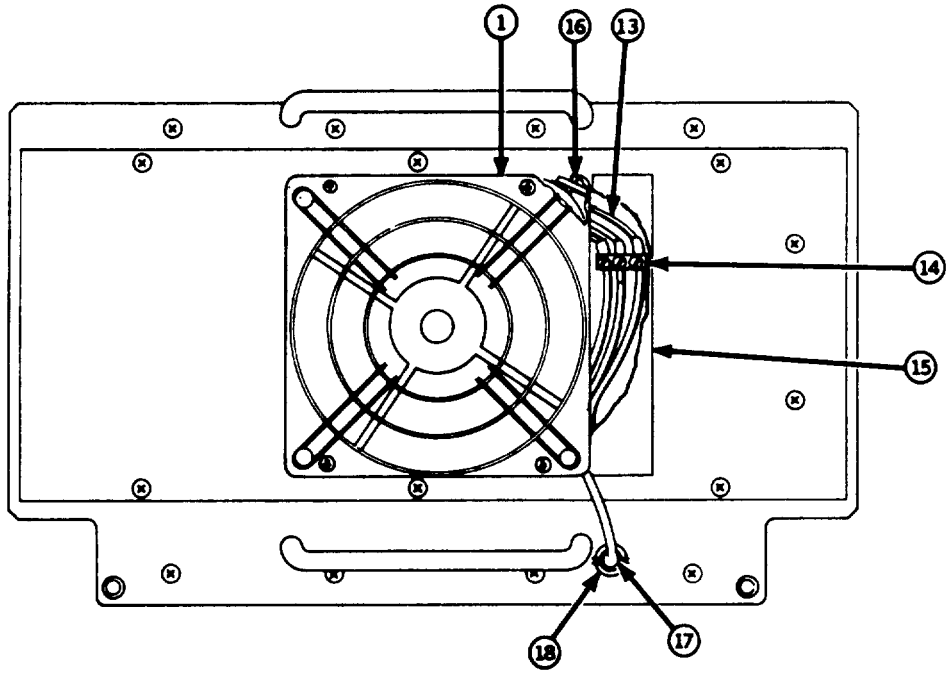
NOTE

Steps 6 thru 8 are for the dc blower fan only.

(6) Install three wires (13) on to terminal strip (14).

(7) Position terminal box (15) on side of blower fan (1). Tighten four captive screws (16).

(8) Install plug (17) in power supply connector (18).



DC BLOWER FAN

EL9JZ146

3-33. POWER UNIT ASSEMBLY REMOVAL AND REPLACEMENT

This procedure is for the ac and dc power unit assemblies. Physical differences are shown in the illustrations.

WARNING

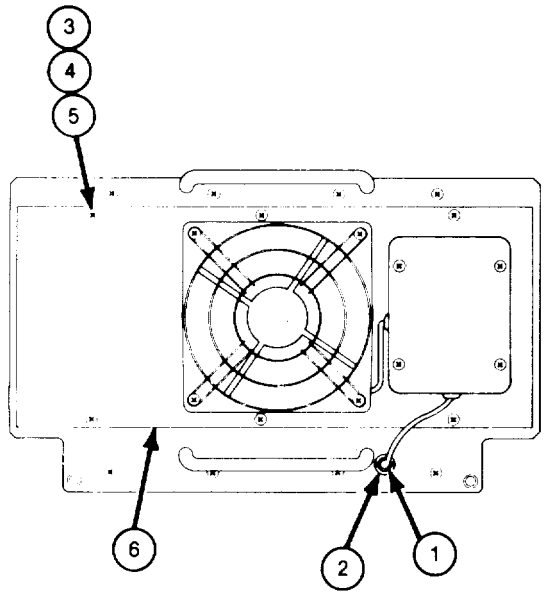
Turn off power before working on equipment. Failure to do so can cause serious injury to personnel.

a. Removal.

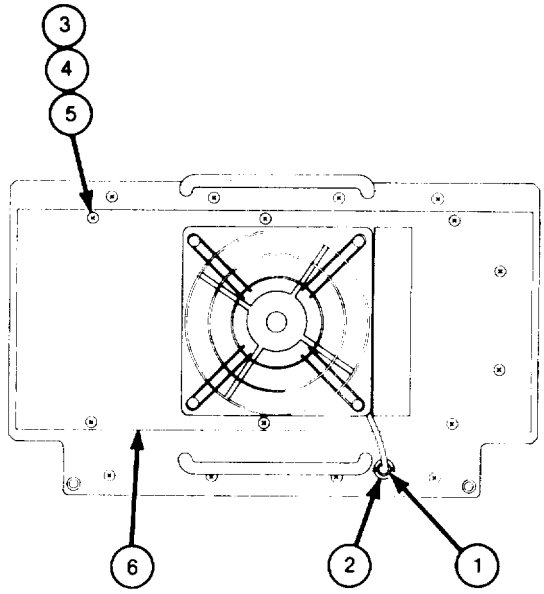
(1) Remove plug (1) from power supply connector (2).

(2) Remove six screws (3), lockwashers (4), and flat washers (5) from power unit assembly (6).

(3) Remove power unit assembly (6).



DC POWER UNIT ASSEMBLY



AC POWER UNIT ASSEMBLY

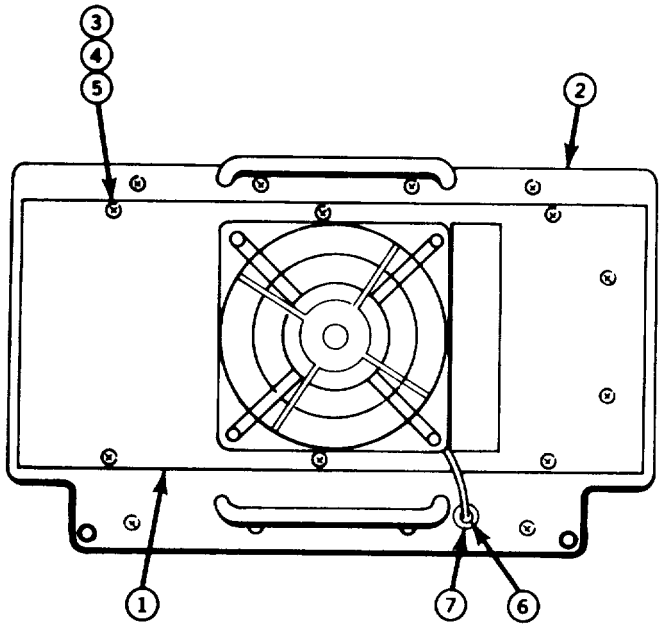
EL9JZ147

b. Replacement.

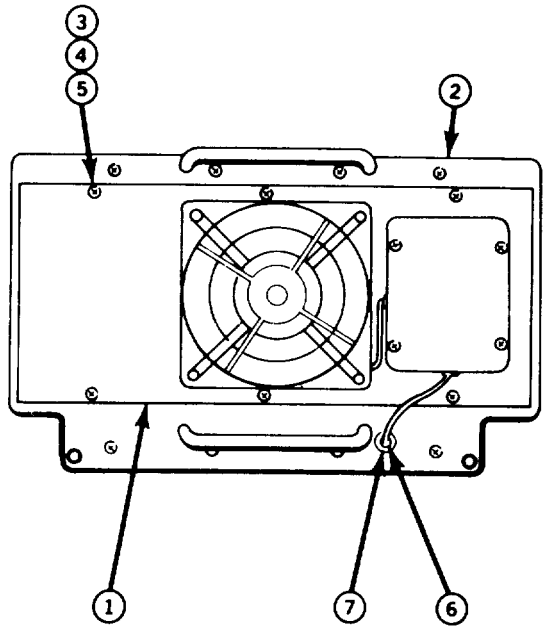
(1) Position power unit assembly (1) on rear of power supply (2).

(2) Install six flat washers (3), lockwashers (4), and screws (5) on power unit assembly (1).

(3) Install plug (6) on power supply connector (7).



DC POWER UNIT ASSEMBLY



AC POWER UNIT ASSEMBLY

EL9JZ148

3-34. POWER SUPPLY REMOVAL AND REPLACEMENT

This procedure is for the semiconductor and core memory processors.

WARNING

Turn off power before working on equipment. Failure to do so can cause serious injury to personnel.

a. Removal.

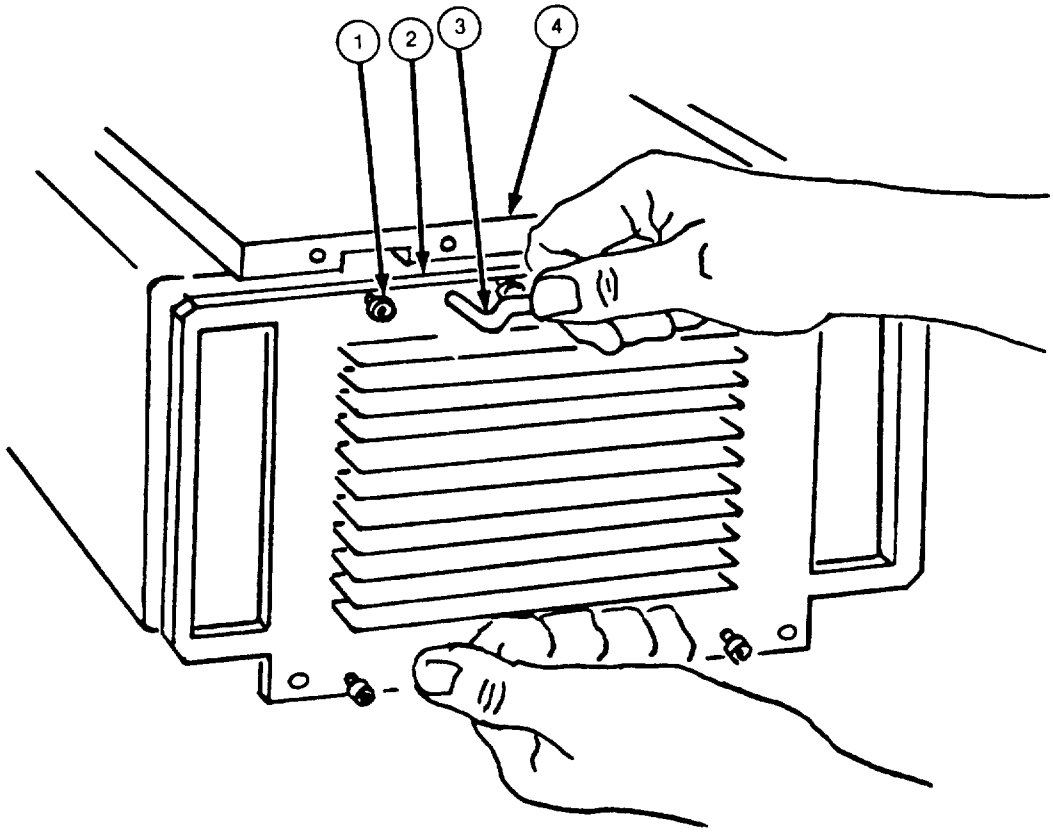
(1) Remove power unit assembly (para 3-33).

(2) Loosen eight captive screws (1) on power supply (2).

CAUTION

Do not rock power supply back and forth when removing it or connector pins will be damaged. Power supply must be pulled straight out of processor.

(3) Grasp two handles (3) and pull power supply (2) straight out of processor (4).



EL9JZ149

b. Replacement.

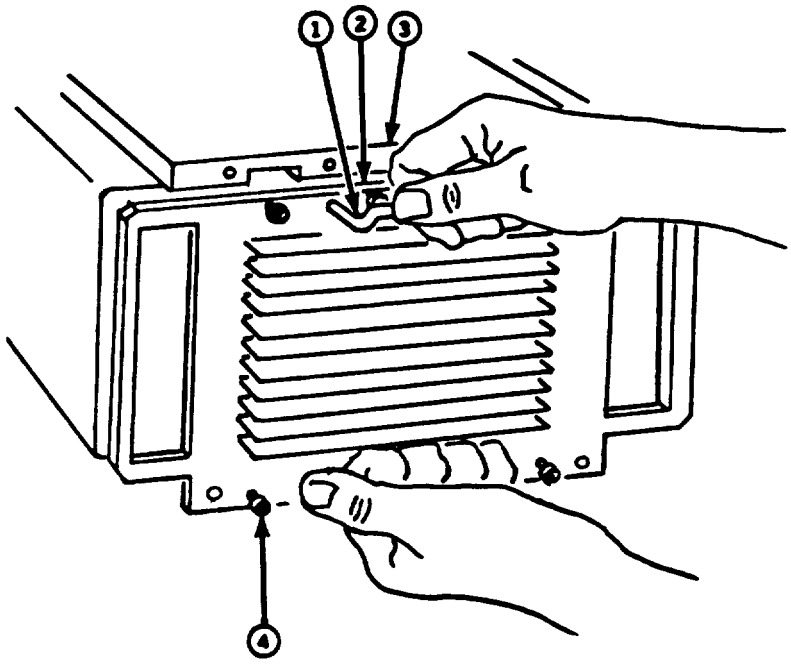
CAUTION

Power supply must be pushed straight into processor or connector pins will be damaged.

(1) Grasp two handles (1), push power supply (2) straight into processor (3).

(2) Tighten eight captive screws (4).

(3) Install power unit assembly (para 3-33).



3-35. EMI FILTER REMOVAL AND REPLACEMENT

This procedure is for the semiconductor and core memory processors.

WARNING

Turn off power before working on equipment. Failure to do so can cause serious injury to personnel.

EL9JZ150

a. Removal.

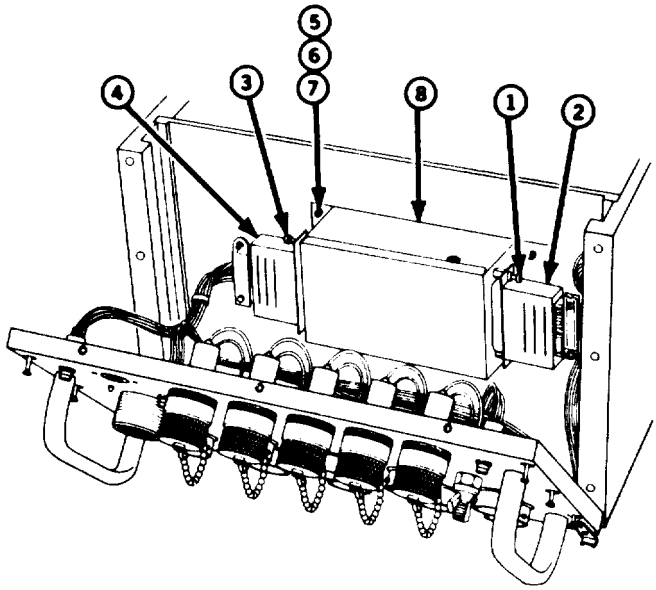
(1) Remove front panel (para 3-30).

(2) Loosen two captive screws (1) and remove connector (2).

(3) Loosen two captive screws (3) and remove connector (4).

(4) Remove four screws (5), Iockwashers (6), and flat washers (7).

(5) Remove EMI filter (8).



b. Replacement.

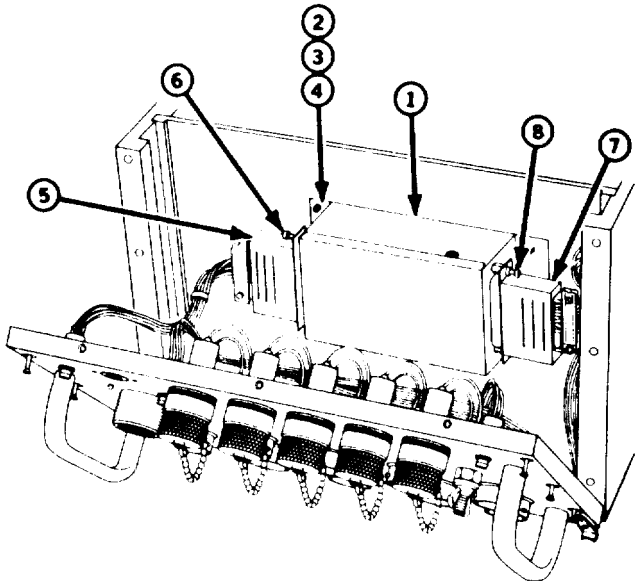
(1) Position EMI filter (1).

(2) Install four flat washers (2), Iockwashers (3), and screws (4).

(3) Install connector (5) and tighten two screws (6).

(4) Install connector (7) and tighten two screws (8).

(5) Install front panel (para 3-30).



EL9JZ151

3-36. FUSE ASSEMBLY REMOVAL AND REPLACEMENT

This procedure is for the semiconductor and core memory processors.

WARNING

Turn off power before working on equipment. Failure to do so can cause serious injury to personnel.

a. Removal.

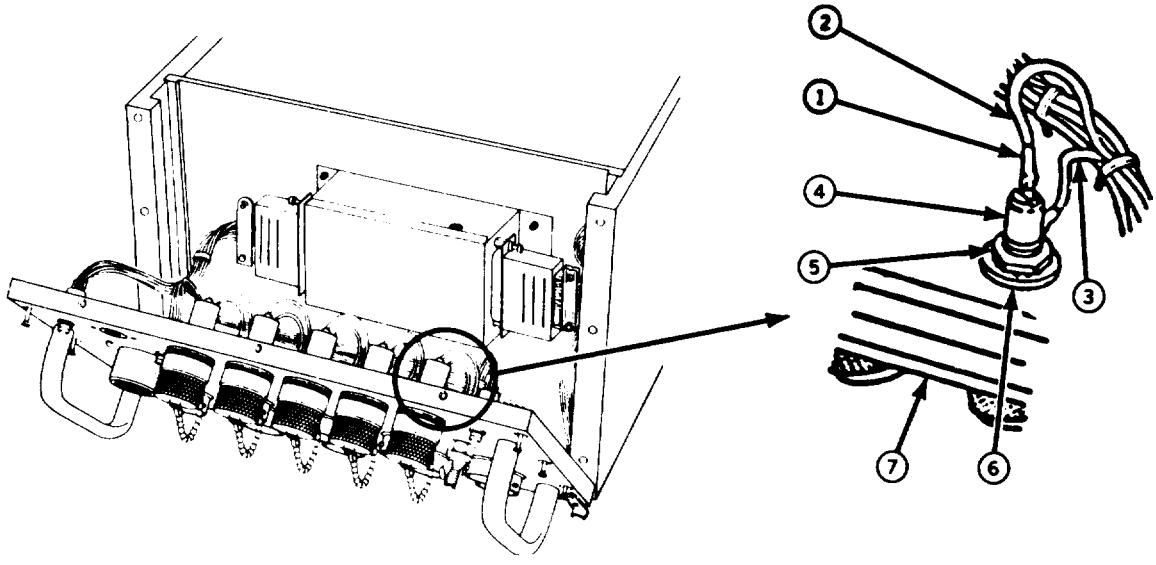
(1) Remove front panel (para 3-30).

(2) Cut and remove heat shrinkable tubing (1) from two wires (2) and (3).

(3) Unsolder and remove two wires (2) and (3) from fuseholder (4). Tag wires.

(4) Remove nut (5) and star washer (6).

(5) Remove fuseholder (4) from front side of panel (7).



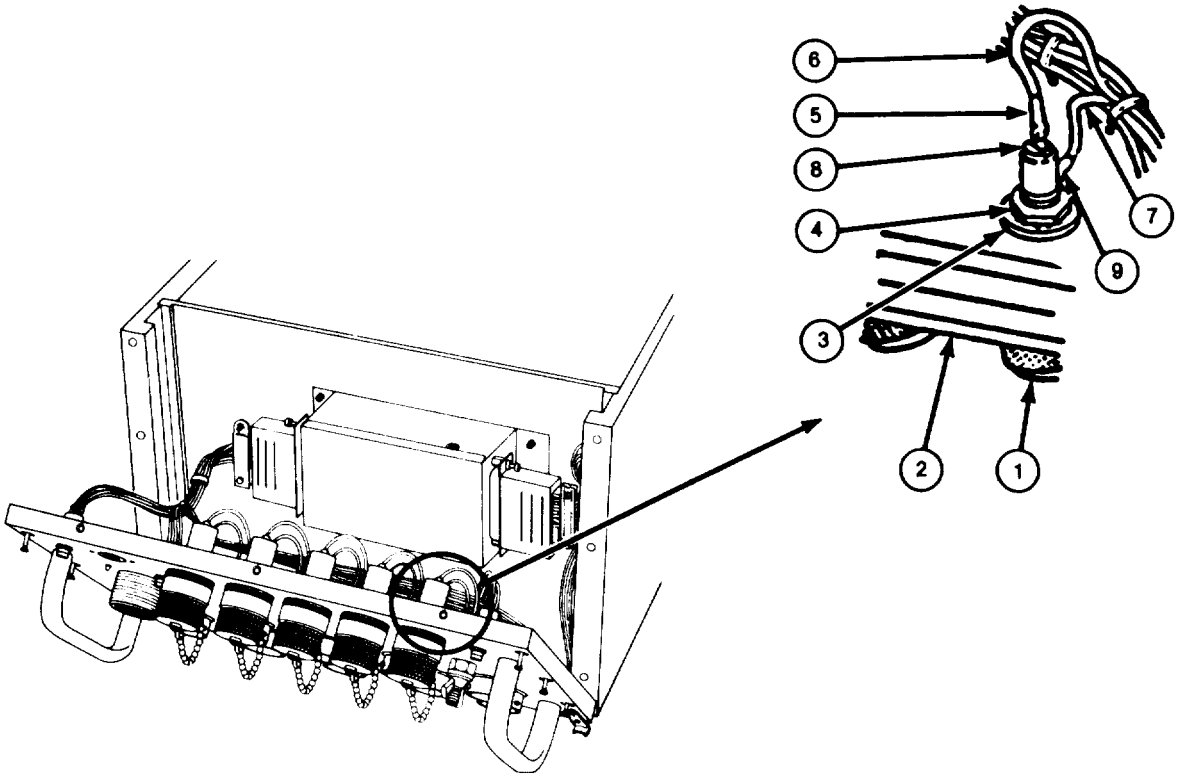
EL9JZ152

b. Replacement.

(1) Position fuseholder (1) on front side of panel (2).

(2) Install star washer (3) and nut (4).

(3) Slide heat shrinkable tubing (5) onto two wires (6) (7).



(4) Solder two wires (6) and (7) onto terminals (8) and (9) on fuseholder (1).

(5) Slide heat shrinkable tubing (5) over terminals (8) and (9).

(6) Apply heat to heat shrinkable tubing (5) until tight on terminals (8) and (9).

(7) Install front panel (para 3-30).

EL9JZ153

3-37. PWR ON/RESET SWITCH REMOVAL AND REPLACEMENT

This procedure is for the semiconductor and core memory processors.

WARNING

Turn off power before working on equipment. Failure to do so can cause serious injury to personnel.

a. Removal.

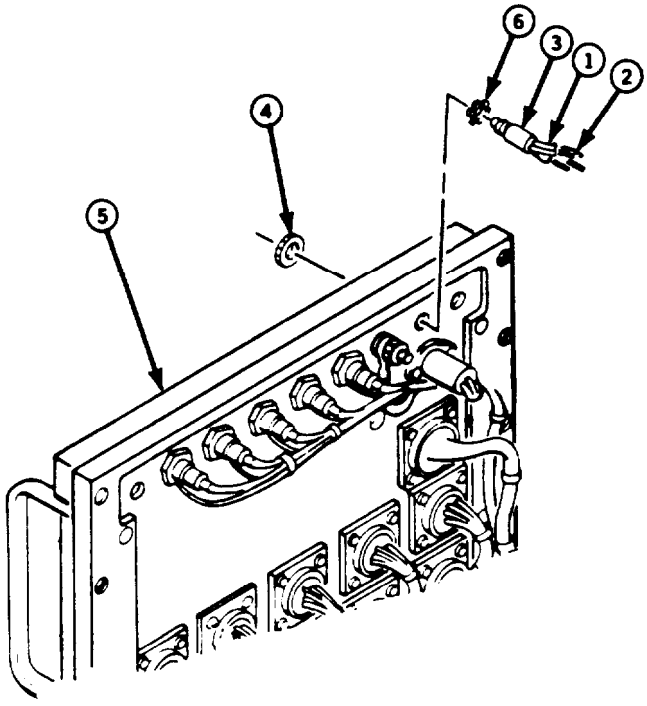
(1) Remove front panel (para 3-30).

(2) Cut and remove heat shrinkable tubing (1) from four wires (2).

(3) Unsolder and remove four wires (2) from PWR ON/RESET switch (3). Tag wires.

(4) Hold switch (3) and remove nut (4).

(5) Remove switch (3) from front panel (5). Remove star washer (6) from switch (3).



EL9JZ164

b. Replacement.

(1) Put star washer (1) on PWR ON/RESET switch (2).

(2) Position switch (2) in front panel (3) and install nut (4).

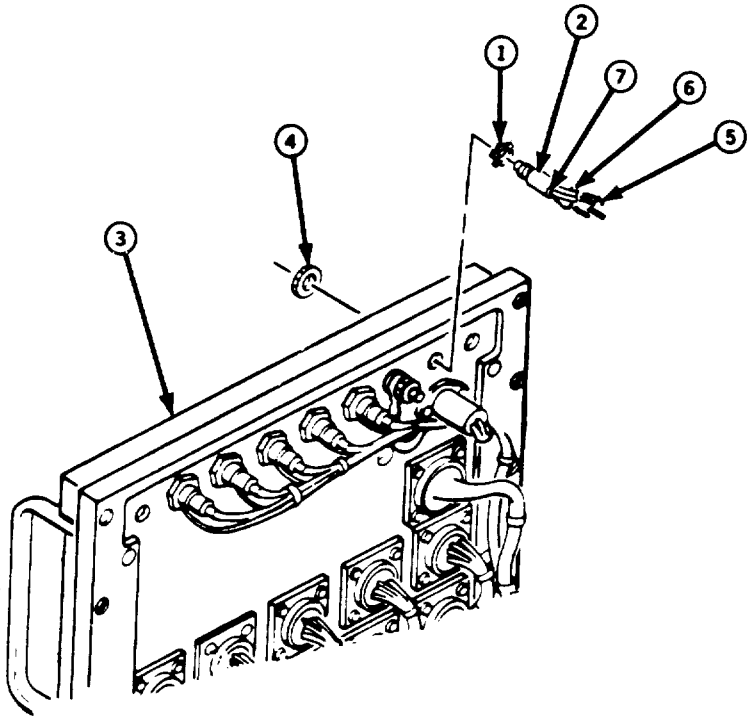
(3) Slide heat shrinkable tubing (6) onto four wires (5).

(4) Solder four wires (5) onto terminals (7) on switch (2).

(5) Slide heat shrinkable tubing (6) over terminals (7).

(6) Apply heat to heat shrinkable tubing (5) until tight on terminals (7).

(7) Install front panel (para 3-30).



EL9JZ155

3-38. ELAPSED TIME METER (ETM) REMOVAL AND REPLACEMENT

This procedure is for the semiconductor and core memory processors. The location Of the indicator differs, as shown in the illustrations.

WARNING

Turn off power before working on equipment. Failure to do so can cause serious injury to personnel.

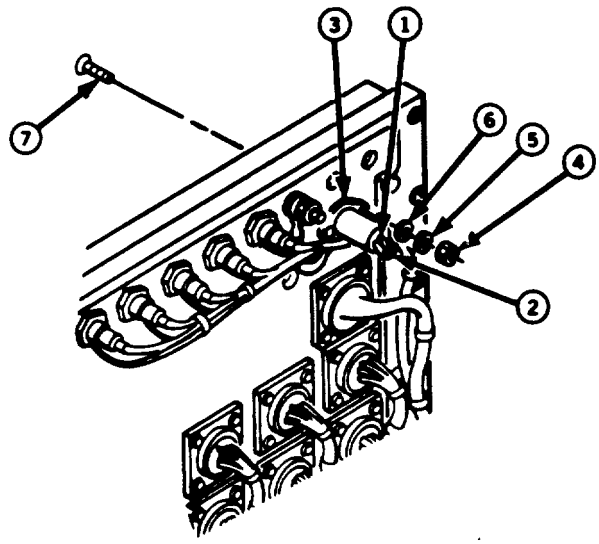
a. Removal.

(1) Remove front panel (para 3-30).

(2) Cut and remove heat shrinkable tubing (1) from three wires (2).

(3) Unsolder and remove three wires (2) from meter (3). Tag wires.

(4) Remove two nuts (4), lockwashers (5), flat washers (6), and screws (7). Remove meter (3).



EQIZ156

b. Replacement.

(1) Position meter (1) on rear of front panel (2).

(2) Install two screws (3), flat washers (4), lockwashers (5), and nuts (6).

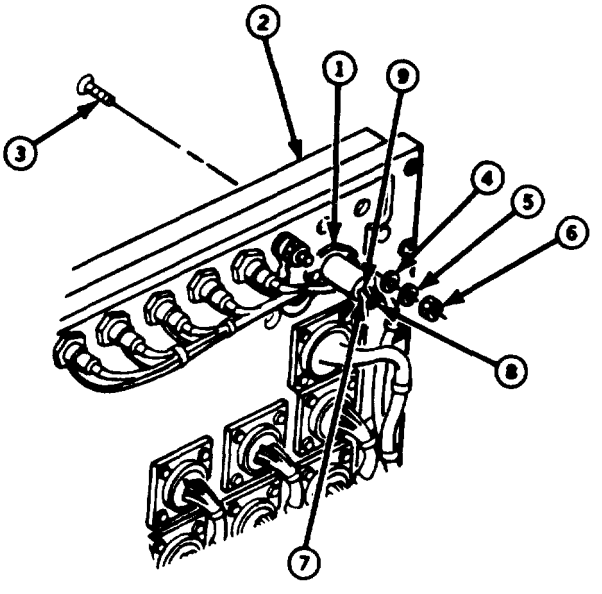
(3) Slide heat shrinkable tubing (7) onto three wires (8).

(4) Solder three wires (8) onto terminals (9) on indicator (1).

(5) Slide heat shrinkable tubing (7) over terminals (9).

(6) Apply heat to heat shrinkable tubing (7) until tight on terminals (9).

(7) Install front panel (para 3-30).



EL9JZ157

3-39. RUN/RESET SWITCH REMOVAL AND REPLACEMENT

This procedure is for the semiconductor and core memory processors.

WARNING

Turn off power before working on equipment. Failure to do so can cause serious injury to personnel.

a. Removal.

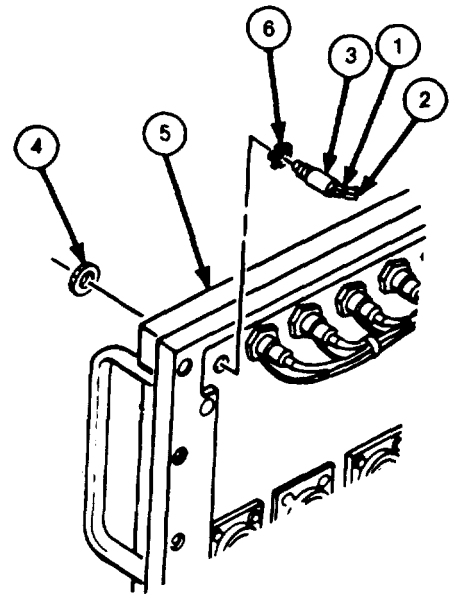
(1) Remove front panel (para 3-30).

(2) Cut and remove heat shrinkable tubing (1) from four wires (2).

(3) Unsolder and remove four wires (2) from RUN/ RESET switch (3). Tag wires.

(4) Hold switch (3) and remove nut (4).

(5) Remove switch (3) from front panel (5). Remove star washer (6) from switch post (7).



EL9JZ158

b. Replacement.

(1) Put star washer (1) on RUN/RESET switch post (2).

(2) Position switch (3) in front panel (4) and install nut (5).

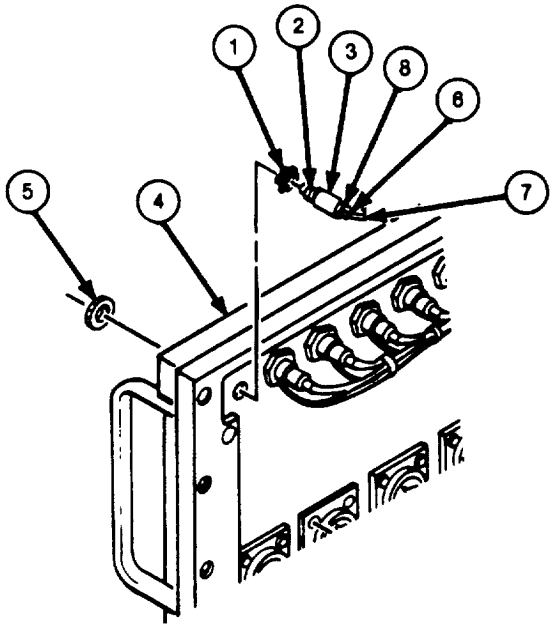
(3) Slide heat shrinkable tubing (6) onto four wires (7).

(4) Solder four wires (7) onto terminals (8) on switch (3).

(5) Slide heat shrinkable tubing (6) over terminals (8).

(6) Apply heat to heat shrinkable tubing (6) until tight on terminals (8).

(7) Install front panel (para 3-30).



3-40. BITE/BOOT SWITCH REMOVAL AND REPLACEMENT

This procedure is for the semiconductor and core memoy processors. The location of the switch differs, as shown in the illustrations.

WARNING

Turn off power before working on equipment. Failure to do so can cause serious injury to personnel.

EL9JZ159

a. Removal.

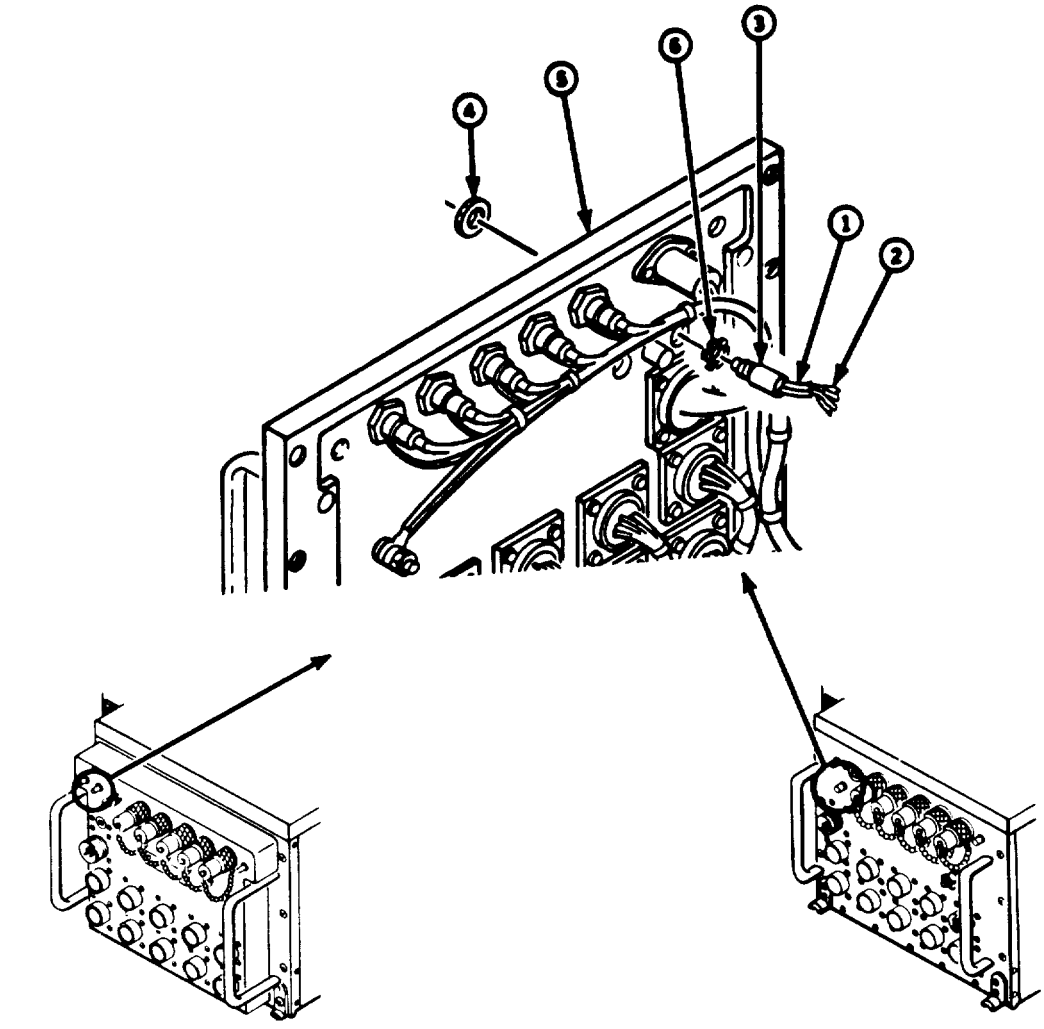
(1) Remove front panel (para 3-30).

(2) Cut and remove heat shrinkable tubing (1) from four wires (2).

(3) Unsolder and remove four wires (2) from BITE/BOOT switch (3). Tag wires.

(4) Hold switch (3) and remove nut (4).

(5) Remove switch (3) from front panel (5). Remove star washer (6) from switch (3).



CORE-BASED PROCESSOR **SEMICONDUCTOR-BASED PROCESSOR**

EL9JZ160

b. Replacement.

(1) Put star washer (1) on BITE/BOOT switch (2).

(2) Position switch (2) in front panel (3) and install nut (4).

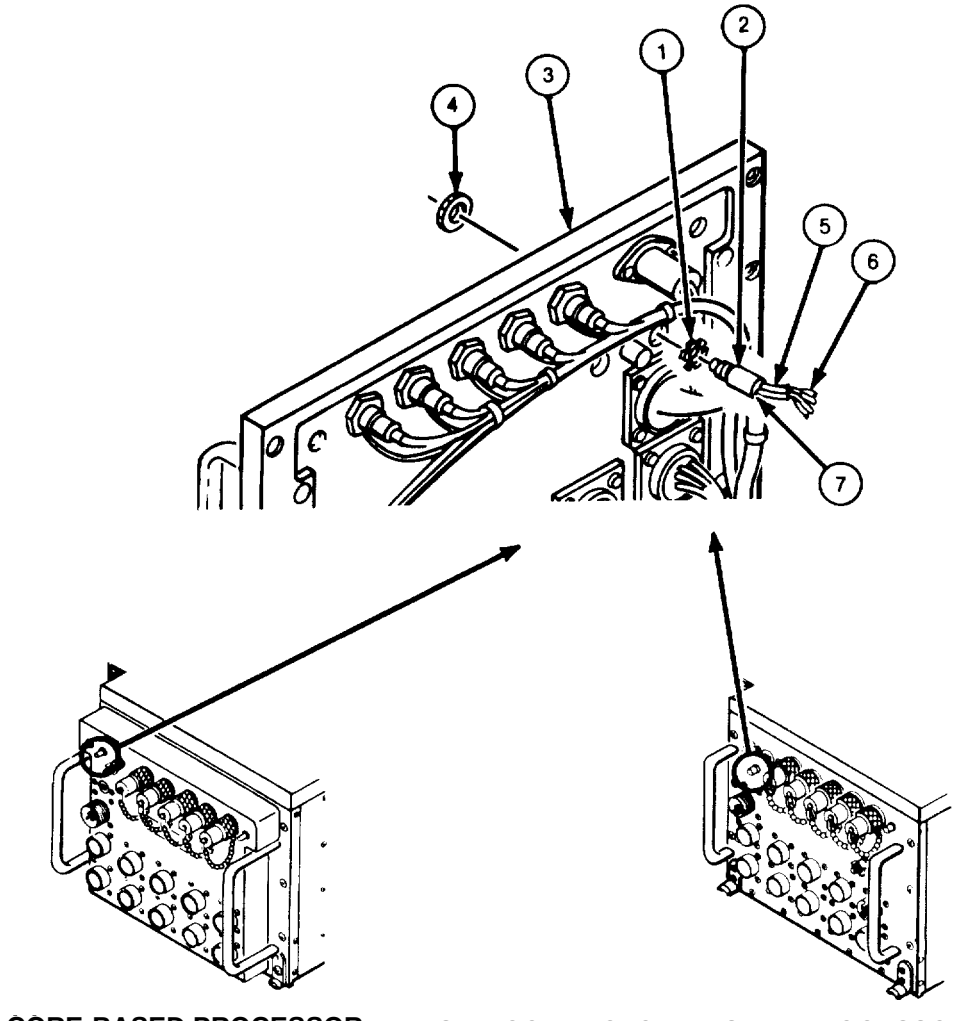
(3) Slide heat shrinkable tubing (5) onto four wires (6).

(4) Solder four wires (6) onto terminals (7) on switch (2).

(5) Slide heat shrinkable tubing (5) over terminals (7).

(6) Using soldering iron, apply heat to heat shirnkable tubing (5) until tight on terminals (7).

(7) Install front panel (para 3-30).



EL9JZ161

3-41. BATT INDICATOR REMOVAL AND REPLACEMENT

This procedure is for the semiconductor processors only.

WARNING

Turn off power before working on equipment. Failure to do so can cause serious injury to personnel.

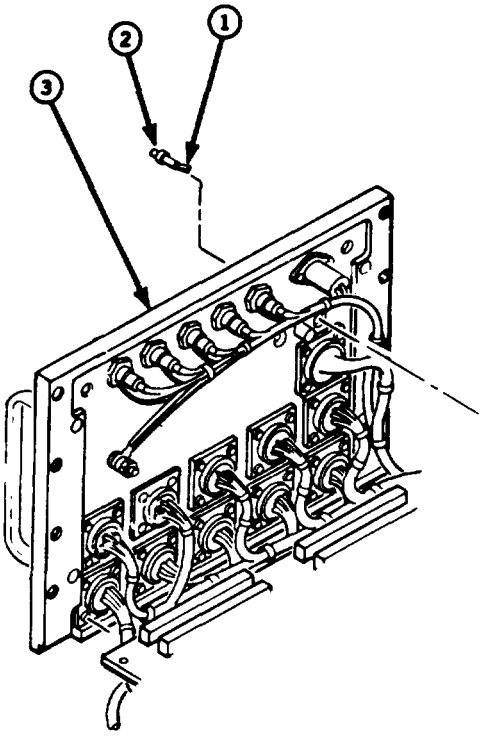
a. Removal.

(1) Remove front panel (para 3-30).

(2) Cut two wires (1) for BAIT indicator (2).

(3) Tag the anode and cathode leads in the processor. Red is anode and black is cathode.

(4) Push BATT indicator (2) out of front panel (3).



EL9JZ162

b. Replacement.

(1) Strip two wire leads (1) on new BATT indicator (2).

(2) Strip two wires (3) in processor.

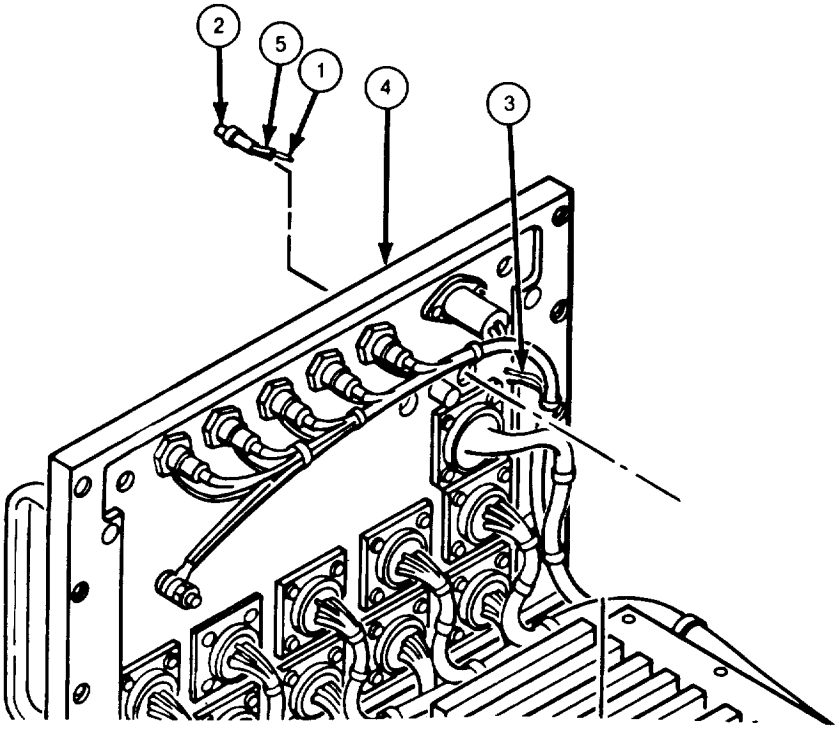
(3) Install BATT indicator (2) in front panel (4).

(4) Slide heat shirnkable tubing (5) onto two wires (3) in processor.

(5) Solder two wire leads (1) to two wires (3). Slide heat shrinkable tubing (5) over soldering joints of wires.

NOTE

Ensure that anode to anode and cathode to cathode connection is made. Red is anode and black is cathode.



(6) Using soldering iron, apply heat to heat shrinkable tubing (5) until it is tight on soldered joints of two wires (1) and wire leads (3).

(7) Install front panel (para 3-30).

3-42. POWER INTERCONNECT HARNESS REMOVAL AND REPLACEMENT

This procedure is for the semiconductor and core memory processors.

WARNING

Turn off power before working on equipment. Failure to do so can cause serious injury to personnel.

a. Removal.

(1) Remove power supply (para 3-34).

(2) Remove top front cover plate (para 3-27).

(3) Remove bottom cover plate (para 3-28).

(4) Remove front panel (para 3-30).

CAUTION

Do not remove heat shrinkable tubing and wires from the connector terminals that are not noted in the procedure and connector wiring diagram.

(5) Cut and remove heat shrinkable tubing (1) from terminals A1, A2 ,3 ,4, 5, 10, 11, and 12 on connector P13 (2).

(6) Unsolder and remove wires (3). Tag wires.

(7) Remove three screws (13) that attach top rear cover plate (14) to power supply bulkhead (10).

(8) Remove six screws (15) that attach top rear cover plate (14) to side panels (6). Remove top rear plate (14).

(9) Remove six screws (4) that attach bottom stiffener (5) to side panel (6).

(10) Remove two screws (7), Iockwashers (8), and washers (9) that attach power supply bulkhead (10) and bottom stiffener (5) to motherboard stiffener (11).

(11) Remove four screws (12) from back side of bottom stiffener (5),

(12) Tilt power supply bulkhead (10) and bottom stiffener (5) forward.

(13) Remove four screws (16) for connector supports (17) from rear of power supply bulkhead (10).

CAUTION

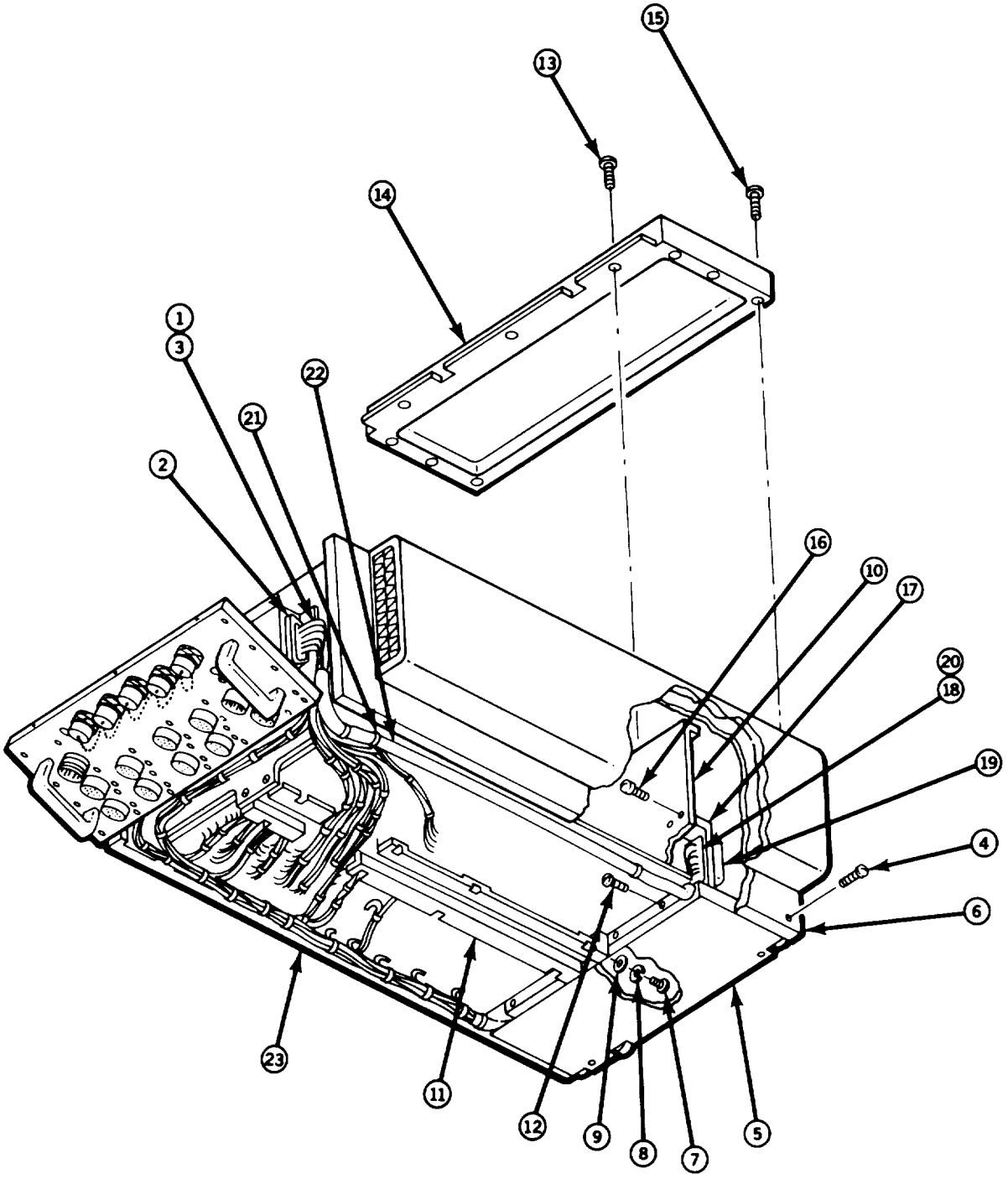
Do not remove heat shrinkable tubing and wires from the connector terminals that are not noted in the procedure and connector wiring diagram.

(14) Cut and remove heat shrinkable tubing (18) from terminals A1, A2, 3, 4, 5, 10, 11, and 12 on connector J14 (19).

(15) Unsolder and remove wires (20). Tag wires.

(16) Cut cable ties (21) that attach power interconnect harness (22) to motherboard (23).

(17) Remove harness (22) through bottom of processor.



EL9JZ164

b. Replacement.

(1) Position harness (1) on motherboard (2).

(2) Install cable ties (3) that were cut to remove harness (1).

(3) Slide heat shrinkable tubing (4) on tagged wires (5) for connector J14 (6).

(4) Solder wires (5) onto connector J14 (6) terminals A1, A2, 3, 4, 5, 10, 11, and 12.

(5) Slide heat shrinkable tubing (4) over terminals.

(6) Apply heat to heat shrinkable tubing (4) until tight on terminals.

(7) Position connector supports (7). Install four screws (8) for connector supports (7) from rear of power supply bulkhead (9).

(8) Position power supply bulkhead (9).

(9) Install four screws (10) on back side of bottom stiffener (11).

(10) Install two washers (12), Iockwashers (13), and screws (14) that attach power supply bulkhead (9) and bottom" stiffener (11) to motherboard stiffener (15).

(11) Install six screws (16) that attach bottom stiffener (11) to side panel (17).

(12) Install six screws (18) that attach bottom top rear cover plate (19) to side panel (17).

(13) Install three screws (20) that attach top rear cover plate (19) to power supply bulkhead (9).

(14) Slide heat shrinkable tubing (21) on tagged wires (22) for connector P13 (23).

(15) Solder wires (22) onto connector P13 (23), terminals A1, A2, 3, 4, 5, 10, 11, and 12.

(16) Slide heat shrinkable tubing (21) over terminals.

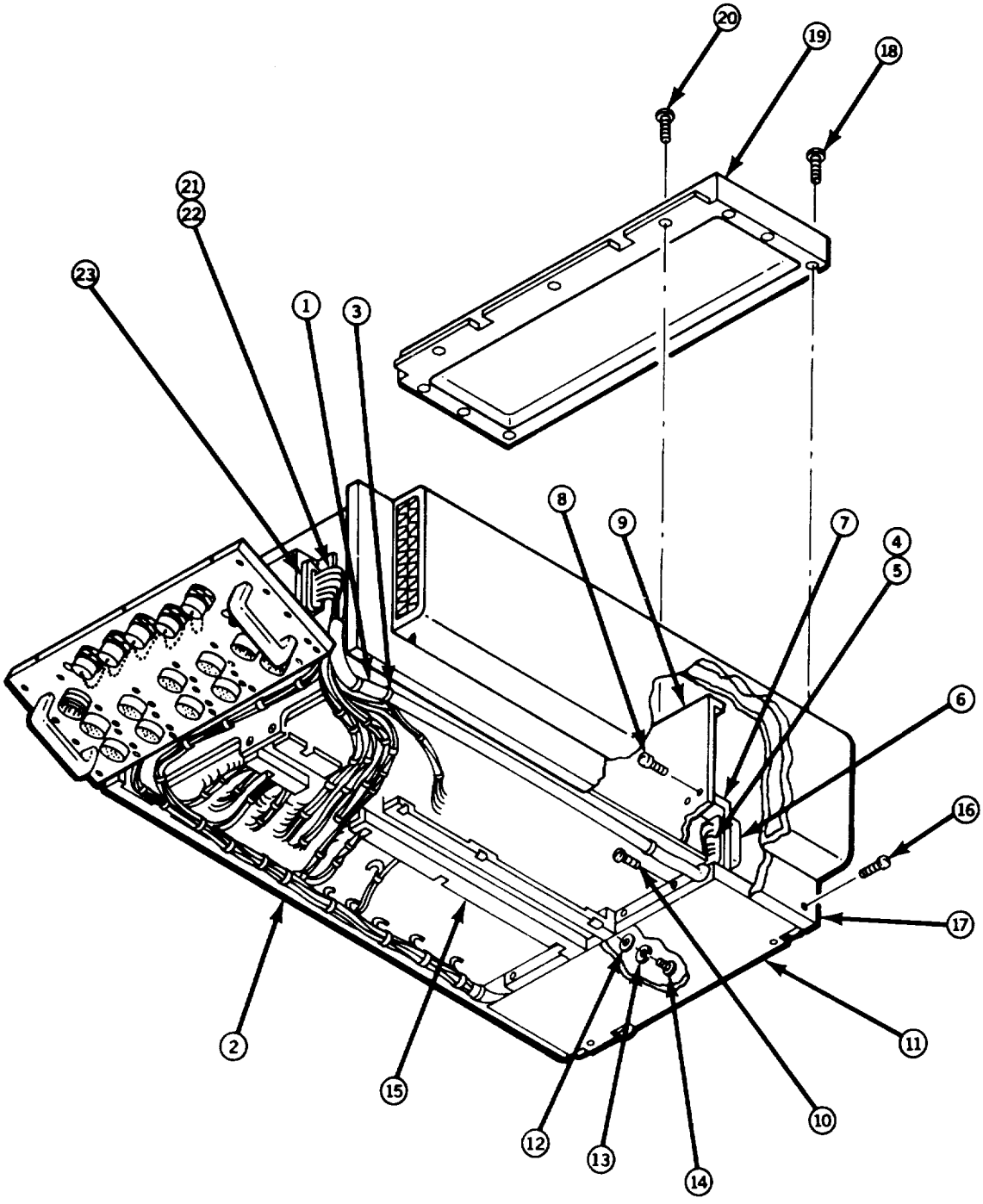
(17) Apply heat to heat shrinkable tubing (21) until tight on terminals.

(18) Install bottom cover plate (para 3-28).

(19) Install top front cover plate (para 3-27).

(20) Install power supply (para 3-34).

(21) Install front panel (para 3-30).



EL9JZ165

3-43. GROUND (GND) STUD REMOVAL AND REPLACEMENT

This procedure is for the semiconductor and core memory processors. The location of the stud differs, as shown in the illustrations.

WARNING

Turn off power before working on equipment. Failure to do so can cause serious injury to personnel.

a. Removal.

(1) Remove front panel (para 3-30).

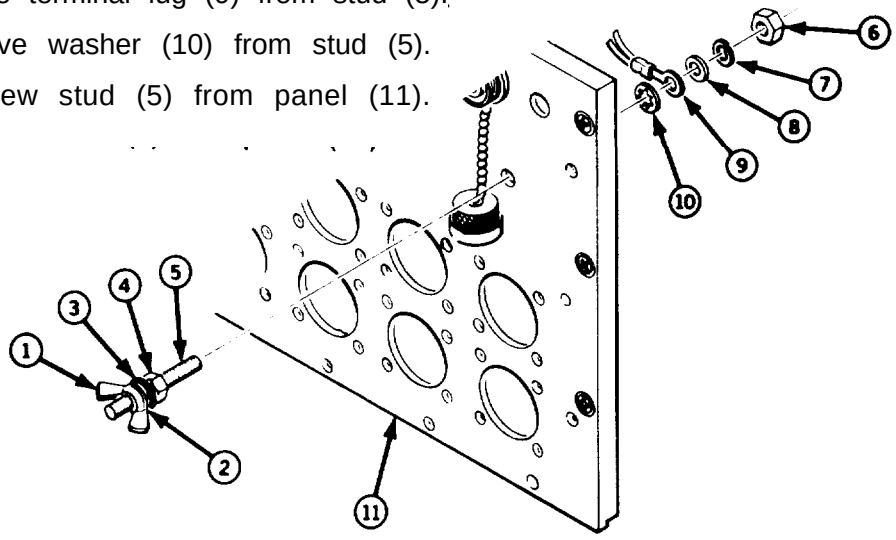
(2) Remove wing nut (1), lockwasher (2), flat washer (3), and nut (4) from stud (5).

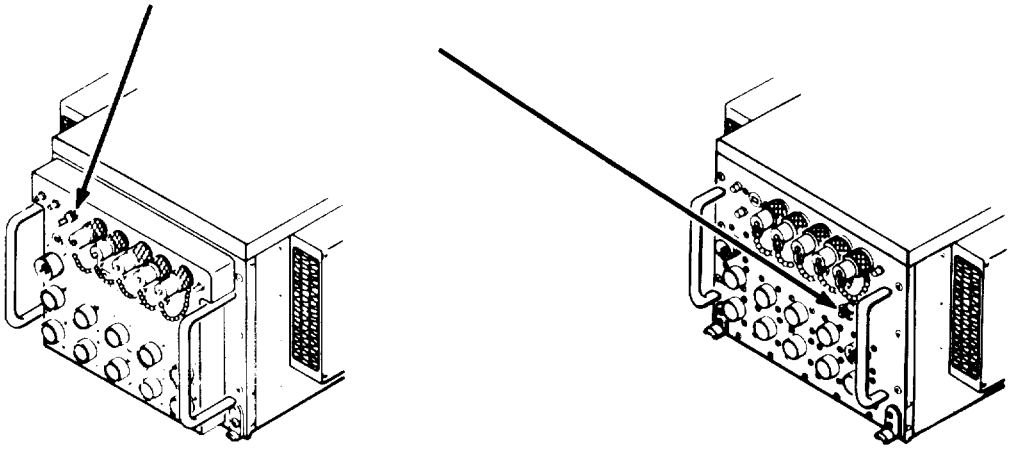
(3) Remove nut (6), lockwasher (7), and flat washer (8) from stud (5).

(4) Remove terminal lug (9) from stud (5).

(5) Remove washer (10) from stud (5).

(6) Unscrew stud (5) from panel (11).





CORE-BASED PROCESSOR

SEMICONDUCTOR-BASED PROCESSOR

EL9JZ166

b. Replacement.

(1) Screw stud (1) into front panel (2).

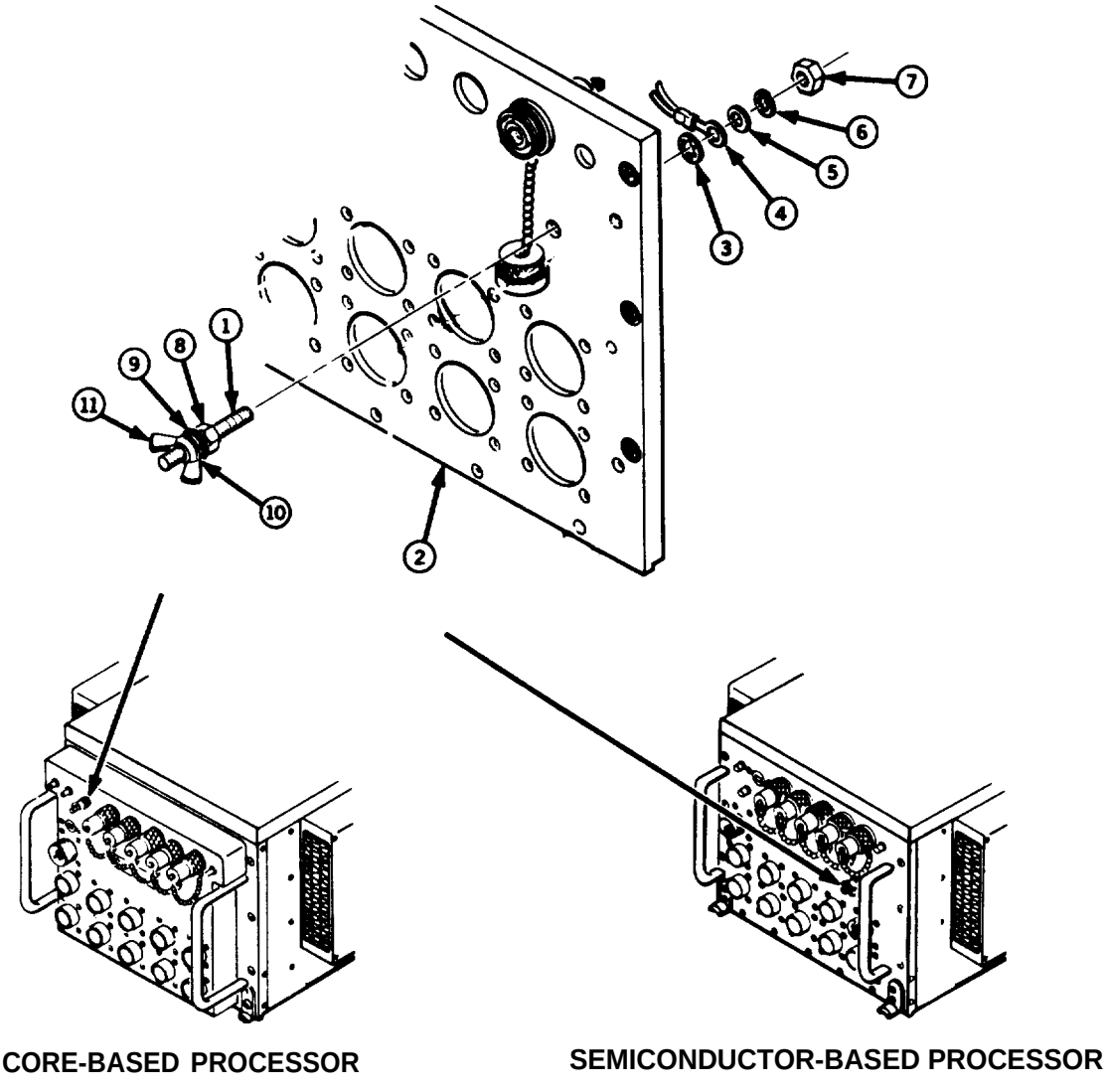
(2) Install washer (3) on stud (1).

(3) Install terminal lug (4) on stud (1).

(4) Install flat washer (5), lockwasher (6), and nut (7) on stud (1).

(5) Install nut (8), flat washer (9), lookwasher (10), and wingnut (11) on stud (1).

(6) Install front panel (para 3-30).



CORE-BASED PROCESSOR **SEMICONDUCTOR-BASED PROCESSOR**

EL9JZ167

3-44. CHASSIS REPLACEMENT

This procedure is for the semiconductor and core memory processors.

WARNING

Turn off power before working on equipment. Failure to do so can cause serious injury to personnel.

a. Removal.

(1) Remove power supply (para 3-34) with power unit assembly attached.

(2) Remove printed circuit boards (PCBs) (para 3-29).

b. Replacement.

(1) Install PCBs (para 3-29).

(2) Install power supply (para 3-34) with power unit assembly attached.

3-45. CERAMIC STANDOFF TERMINAL REPLACEMENT

This procedure is for the semiconductor and core memory processors.

WARNING

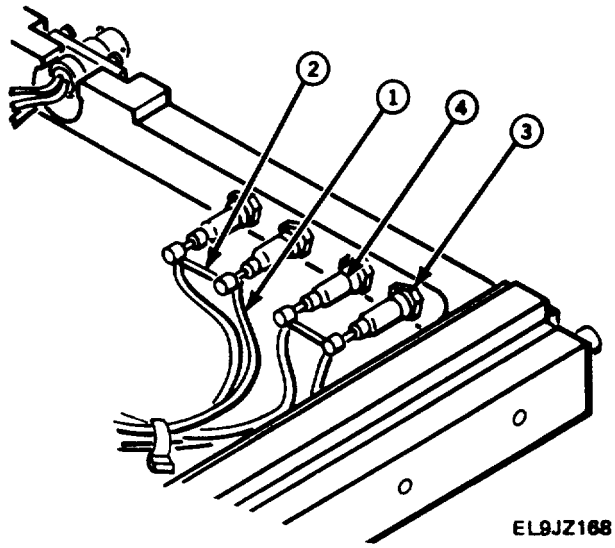
Turn off power before working on equipment. Failure to do so can cause serious injury to personnel.

a. Removal.

(1) Remove power supply (para 3-34).

(2) Unsolder and remove lead wire (1) and jumper wire (2).

(3) Unscrew nut (3) and remove ceramic standoff terminal (4).

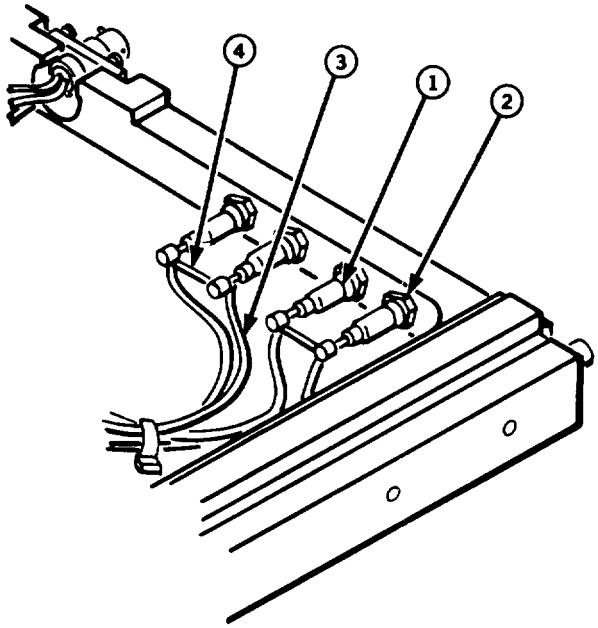


b. Replacement.

(1) Aline ceramic standoff terminal (1) and nut (2) in position. Tighten nut (2).

(2) Solder lead wire (3) and jumper wire (4) to terminal (1).

(3) Install power supply (para 3-34).



EL9JZ169

3-46. FRONT PANEL HANDLES REMOVAL AND REPLACEMENT

This procedure is for either front panel handle on the semiconductor or core memory processors.

a. Removal.

(1) Remove front panel (para 3-30).

(2) Remove two screws (1) from rear of panel (2).

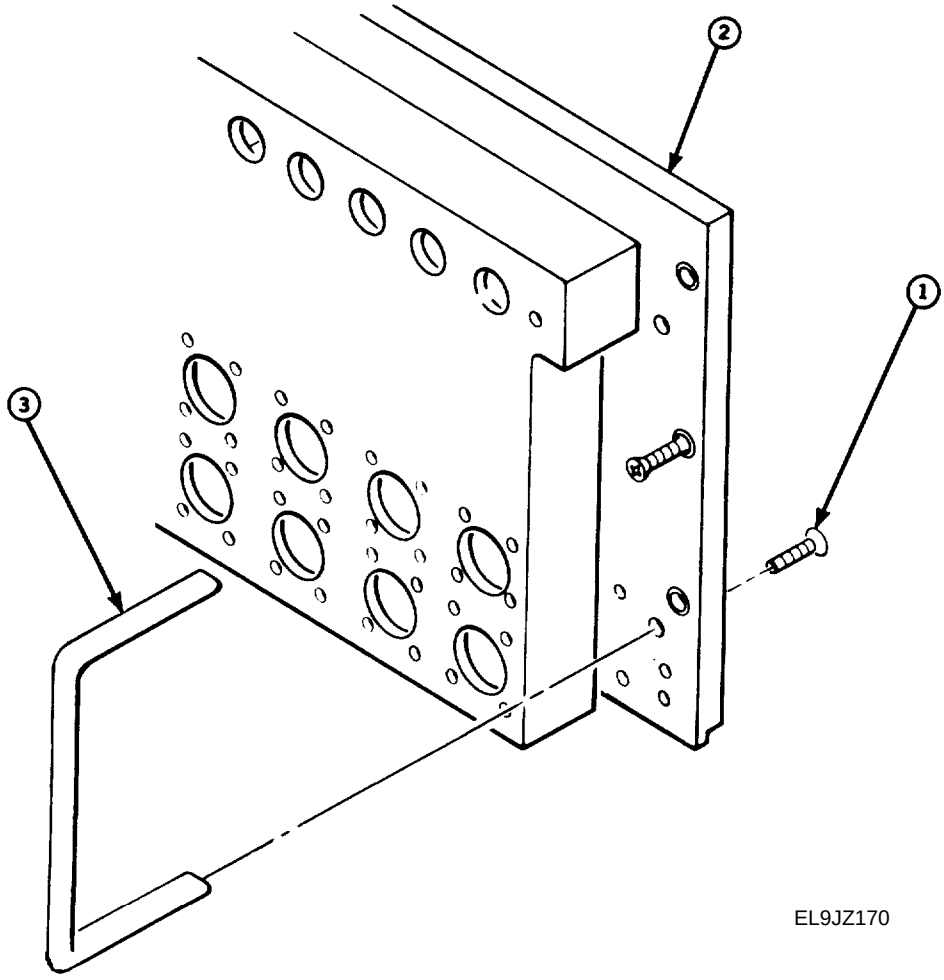
(3) Remove handle (3) from panel (2).

b. Replacement.

(1) Position handle (3) on front panel (2).

(2) Install two screws (1) into handle (3) from rear of panel (2).

(3) Install front panel (para 3-30).



3-47. POWER SUPPLY HANDLES REMOVAL AND REPLACEMENT

This procedure is for either power supply handle on the semiconductor or core memory processors.

a. Removal.

(1) Remove power supply (para 3-34).

(2) Remove two screws (1) from rear of handle (2).

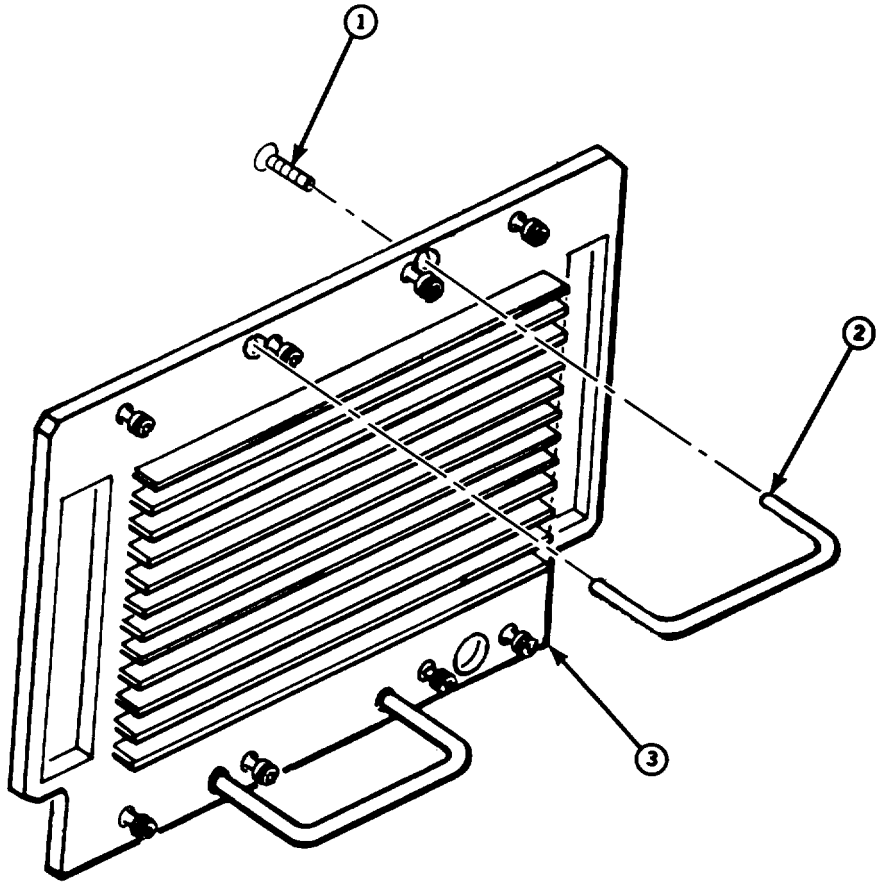
(3) Remove handle (2) from power supply (3).

b. Replacement.

(1) Position handle (2) on power supply (3).

(2) Install two screws (1) into handle (2).

(3) Install power supply (para 3-34).



EL9JZ171

Section VI. REPAIR PROCEDURES

3-48. INTRODUCTION

This section provides procedures for repairing the processor and its components that are serviceable at direct support maintenance. Differences between the core- and semiconductor-based processors, as applicable to repairs, are noted in the repair procedures to follow.

3-49. I/O CABLE REPAIR

This procedure is for all cables connecting the I/O chassis to the semiconductor or core memory processor.

WARNING

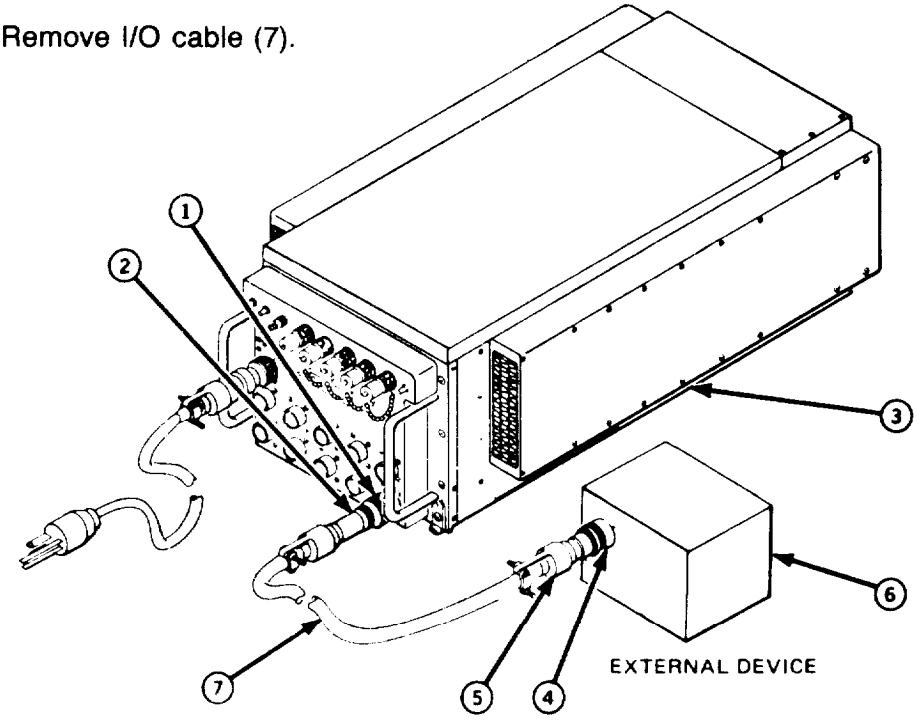
Turn off power before working on equipment. Failure to do so can cause serious injury to personnel.

a. Removal.

(1) Turn knurled ring (1) to the left and remove connector (2) from processor (3),

(2) Turn knurled ring (4) to the left and remove connector (5) from I/O chassis (6).

(3) Remove I/O cable (7).

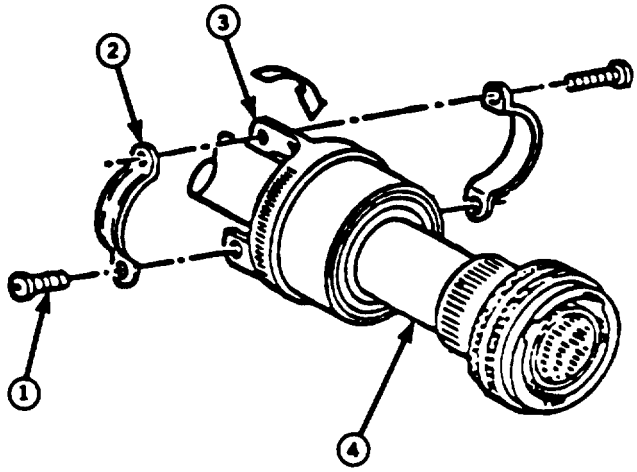


EL9JZ172

b. Repair.

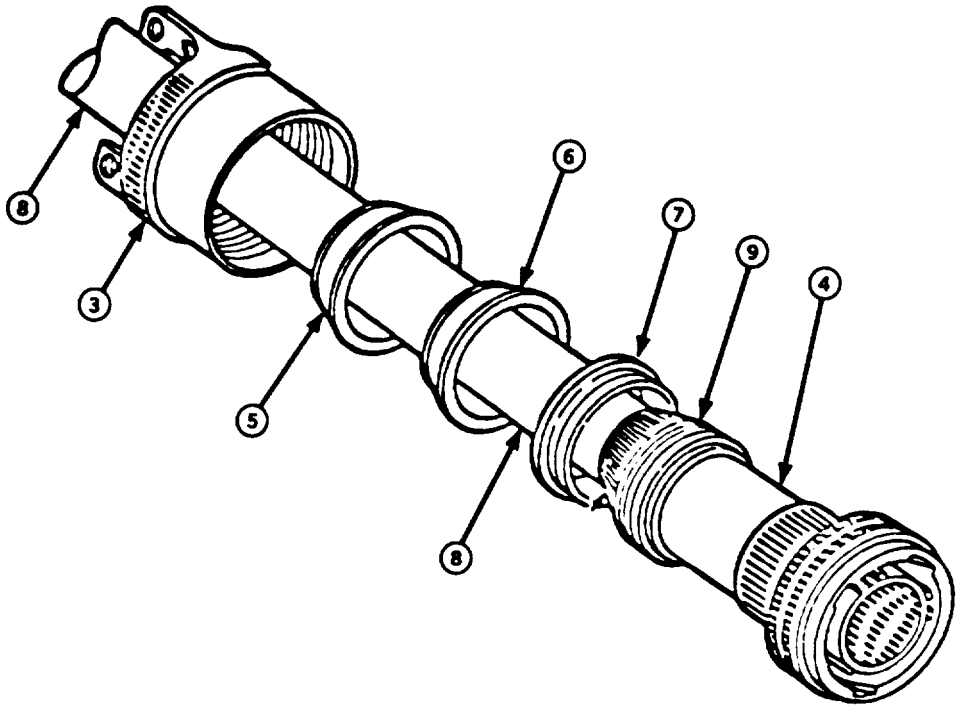
(1) Remove two screws(1) and two retainers (2) from flange (3).

(2) Hold sleeve (4) and turn flange (3) in direction of arrow to unscrew.



(3) Slide flange (3), metal collar (5), rubber collar (6), and grounding ring (7) back on cable (8).

(4) Roll back cable shield (9) from narrow end of sleeve (4) and flatten on cable (8).



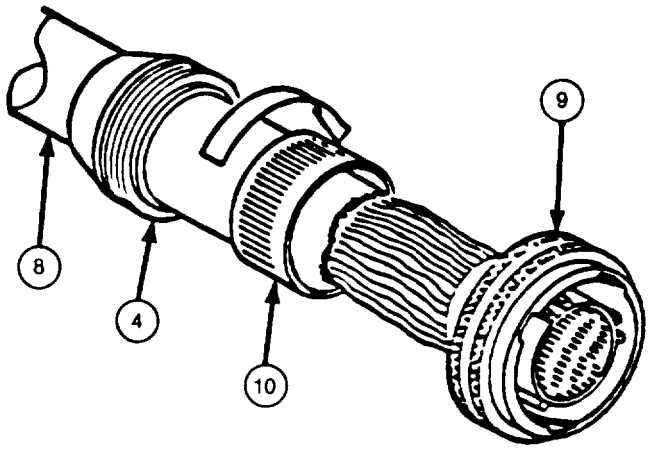
EL9JZ173

(5) Install connector (9) on a mating receptacle.

(6) Hold receptacle and turn knurled ring (10) on sleeve (4) in direction of arrow and separate sleeve from connector (9). Remove connector from receptacle.

(7) Slide sleeve (4) back on cable (8).

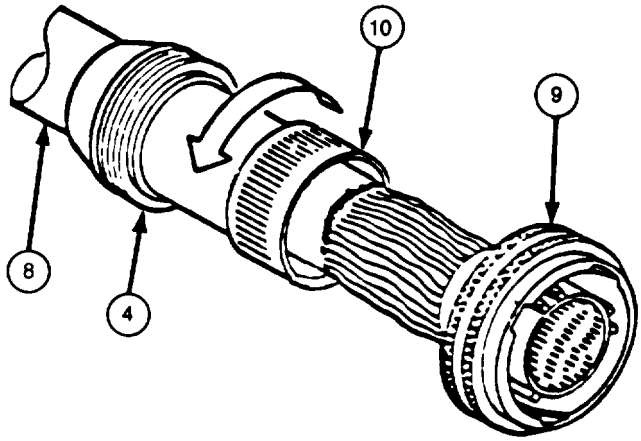
(8) Replace damaged pin (para 3-51).



(9) Slide sleeve (4) forward on cable (8) to connector (9).

(10) Install connector (9) on a mating receptacle.

(11) Hold receptacle and turn knurled ring (10) on sleeve (4) in direction of arrow. Remove connector from receptacle.

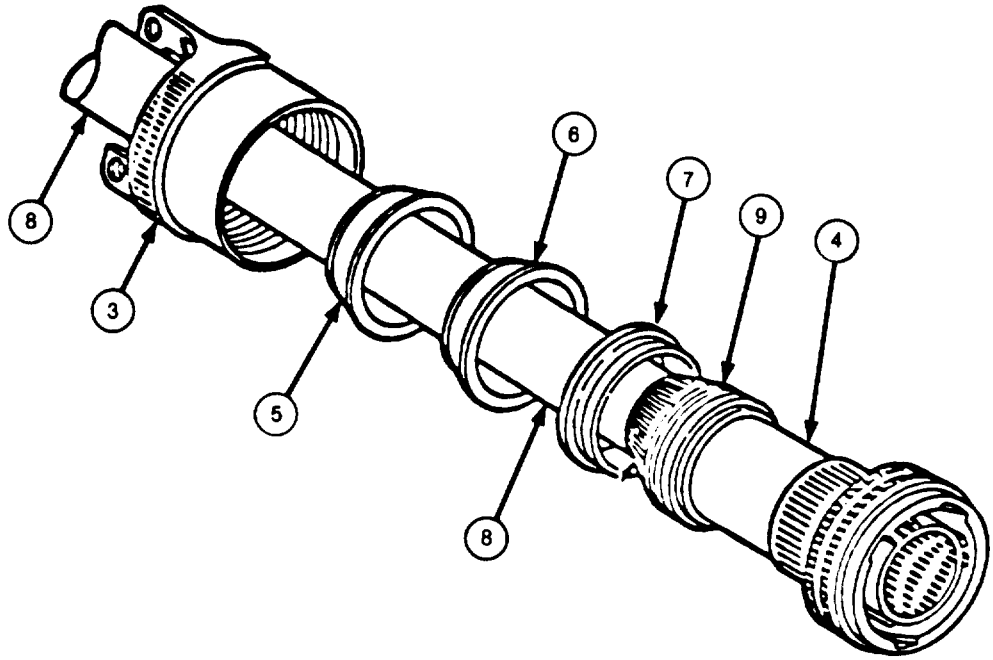


EL9.JZ174

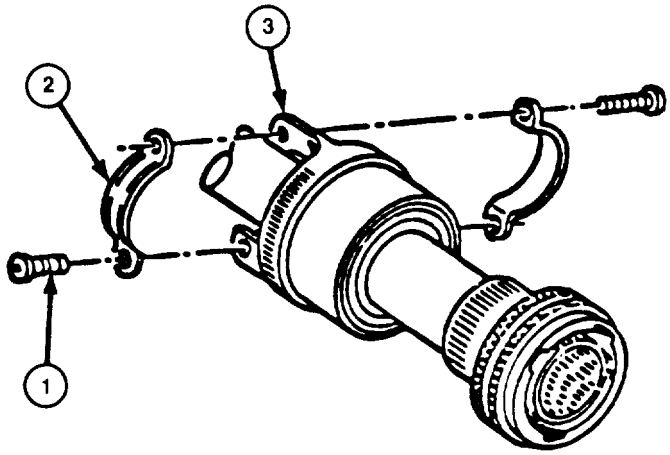
(12) Remove any cable shield (9) from under sleeve (4) and fold over end of sleeve.

(13) Slide flange (3) with metal collar (5), rubber collar (6), and grounding ring (7) over sleeve (4).

(14) Hold sleeve (4) and screw flange (3) onto sleeve (4) by turning it in direction of arrow.



(15) Install two retainers (2), with two screws (1) on flange (3).



EL9JZ175

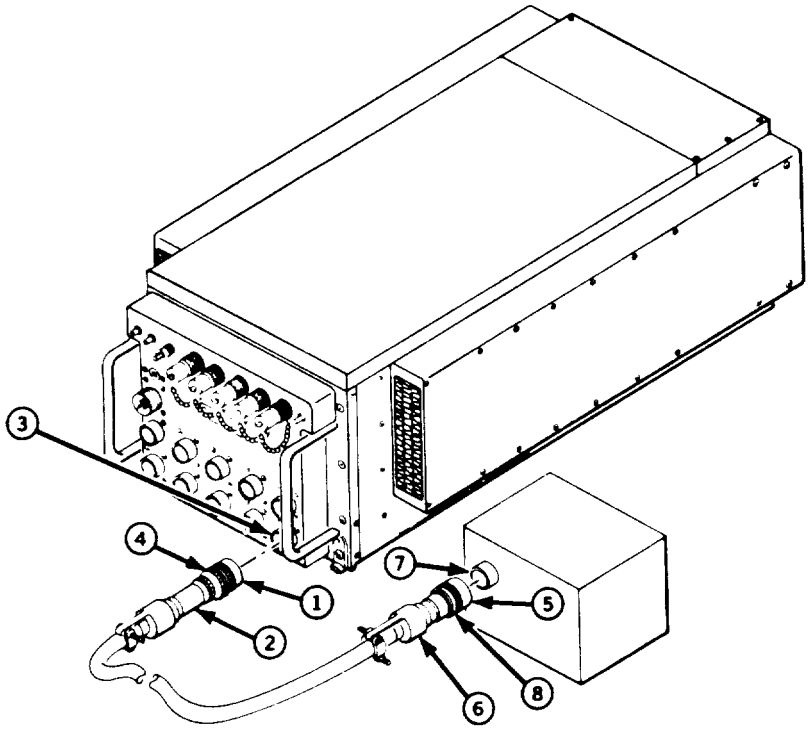
c. Replacement.

(1) Aline tabs (1) on cable connector (2) with slots on processor connector (3).

(2) Turn knurled ring (4) to the right until it clicks into place.

(3) Aline tabs (5), on cable connector (6) with slots on I/O chassis connector (7).

(4) Turn knurled ring (8) to the right until it clicks into place.



3-50. POWER CABLE REPAIR

This procedure is for the semiconductor and core memory processors.

WARNING

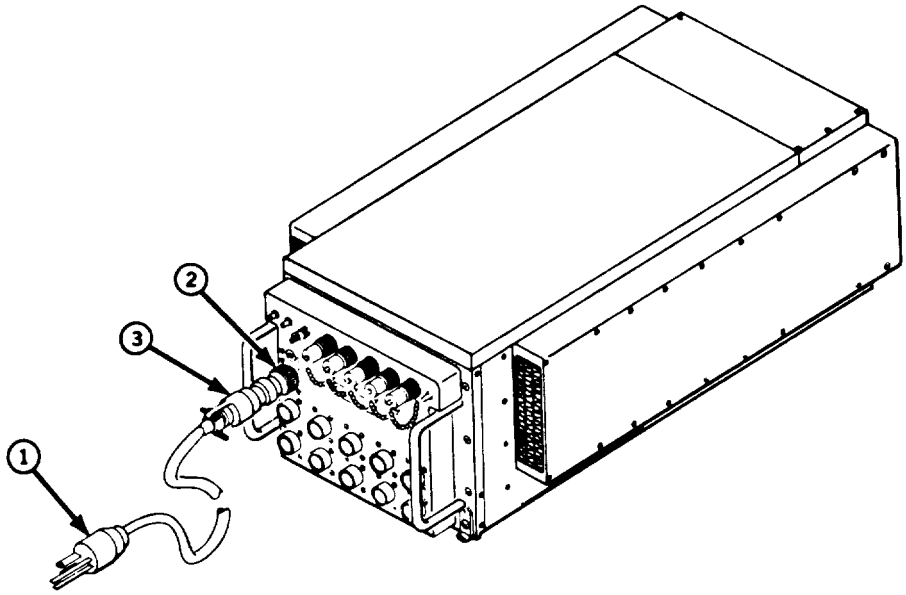
Turn off power before working on equipment. Failure to do so can cause serious injury to personnel.

EL9JZ176

a. Removal.

(1) Remove plug (1) from power source.

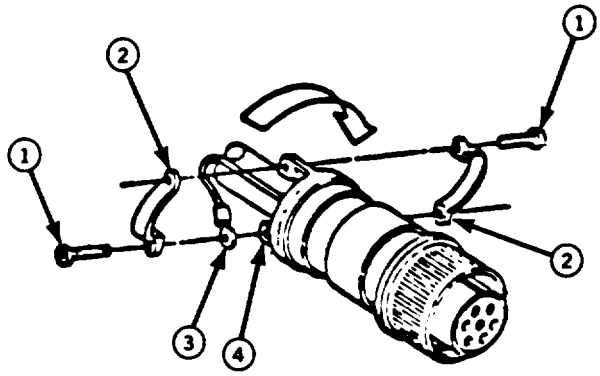
(2) Turn knurled ring (2) to the left and remove power cable (3).



b. Repair Connector).

(1) Remove two screws (1) and two retainers (2), and ground wire (3) from flange (4).

(2) Unscrew flange (4) in direction of arrow.



EL9JZ177

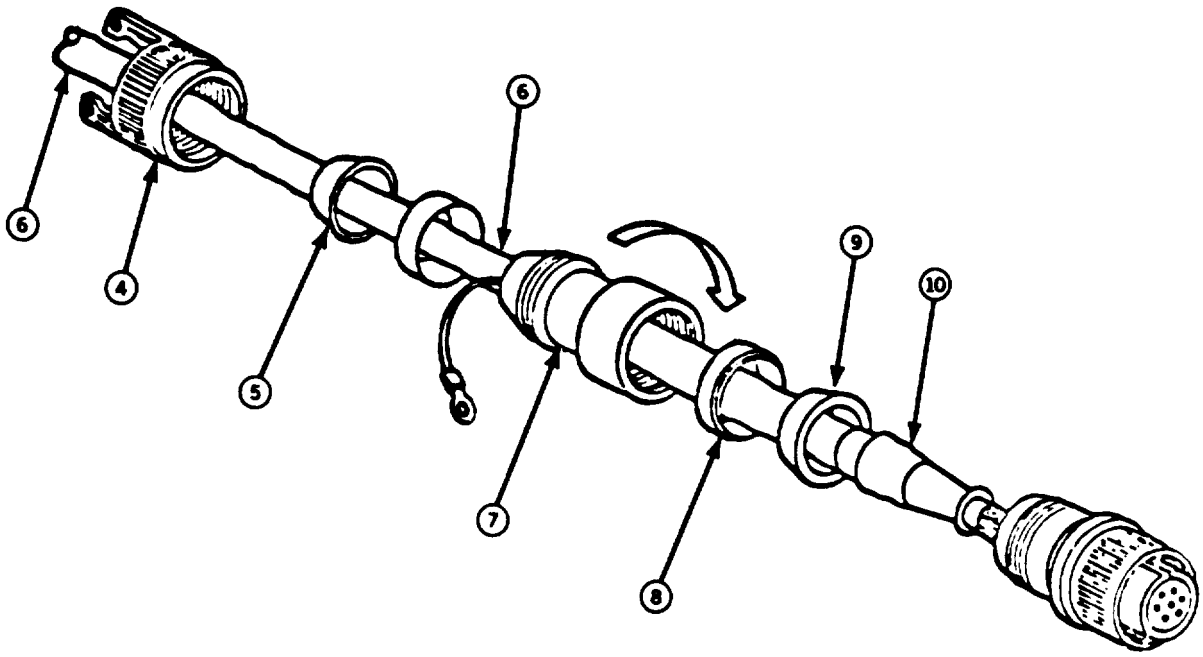
(3) Slide flange (4) and two metal collars (5), back on cable (6).

(4) Unscrew sleeve (7) in direction of arrow.

(5) Slide sleeve (7), metal collar (8), and rubber collar (9) back on cable (6).

(6) Slide boot (10) back on cable (6).

(7) Replace damaged socket inserts (para 3-51).



EL9JZ178

(8) Slide boot (10) forward on cable to cover exposed wire leads (11).

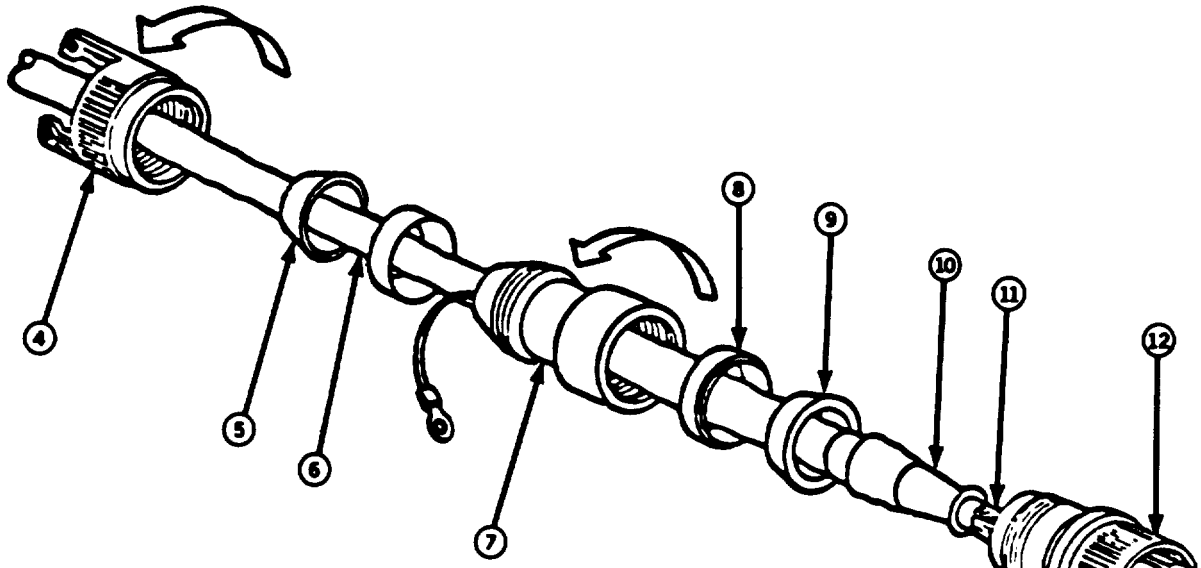
(9) Slide rubber collar (9) up to connector (12).

(10) Slide metal collar (8) up to rubber collar (9).

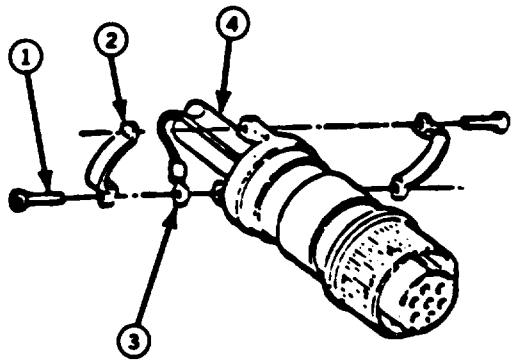
(11) Slide sleeve (7) over collars (8), (9). Screw on sleeve (7) by turning it in direction of arrow.

(12) Slide two metal collars (5) and flange (4) forward on cable (6).

(13) Screw on flange (4) by turning it in direction of arrow.



(14) Install two screws (1), two retainers (2), and ground wire (3) on flange (4).



EL9JZ179

c. Repair (Plug).

NOTE

Repair of plug consists of removing damaged one and installing new one.

(1) Loosen three captive screws (1).

(2) Remove two screws (2) on plug clamp (3). Remove plug clamp (3).

(3) Separate plug (4), as shown.

(4) Tag three wires (5).

(5) Loosen three screws (6) and remove three wires (5).

(6) Remove and discard plug (4).

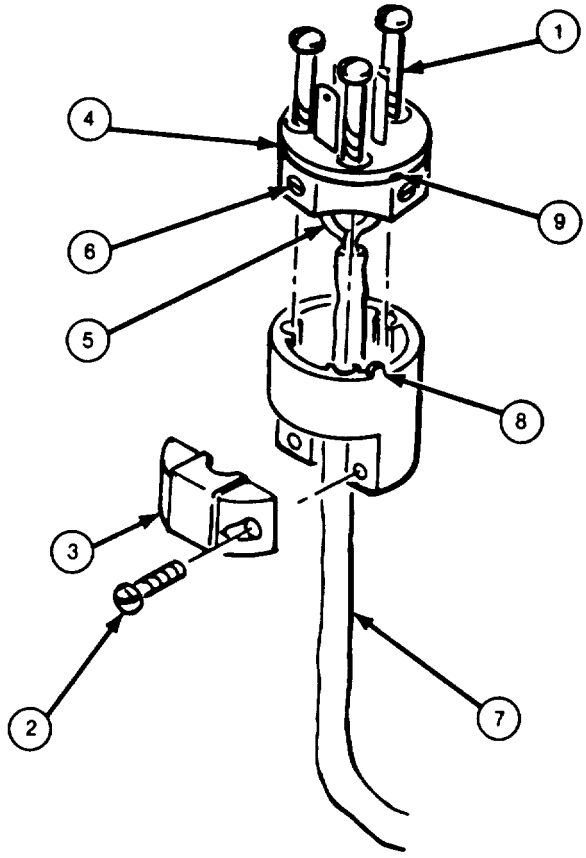
(7) Put new plug (4) over cable (7), as shown.

(8) Insert wires (5) in plug (4), as tagged, and tighten three screws (6). Remove tags.

(9) Aline tab (8) on lower section of plug (4) with slot (9) on upper section of plug.

(10) Join sections of plug (4), aline and tighten three captive screws (1).

(11) Position plug clamp (3) and install two screws (2).



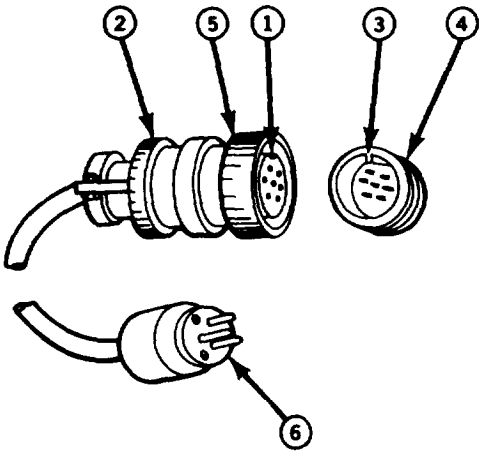
EL9JZ180

d. Replacement.

(1) Aline slot (1) on cable connector (2) with key (3) on processor connector (4).

(2) Turn knurled ring (5) to the right.

(3) Connect plug (6) to power source.



EL9JZ190

3-51. FRONT PANEL CONNECTOR REPAIR

This procedure is for front panel connectors J2 through J5 and J7 through J11 on the semiconductor processor, and J2 through J6 and J7 through J11 on the core memory processor.

WARNING

Turn off power before working on equipment. Failure to do so can cause serious injury to personnel

a. Removal.

NOTE

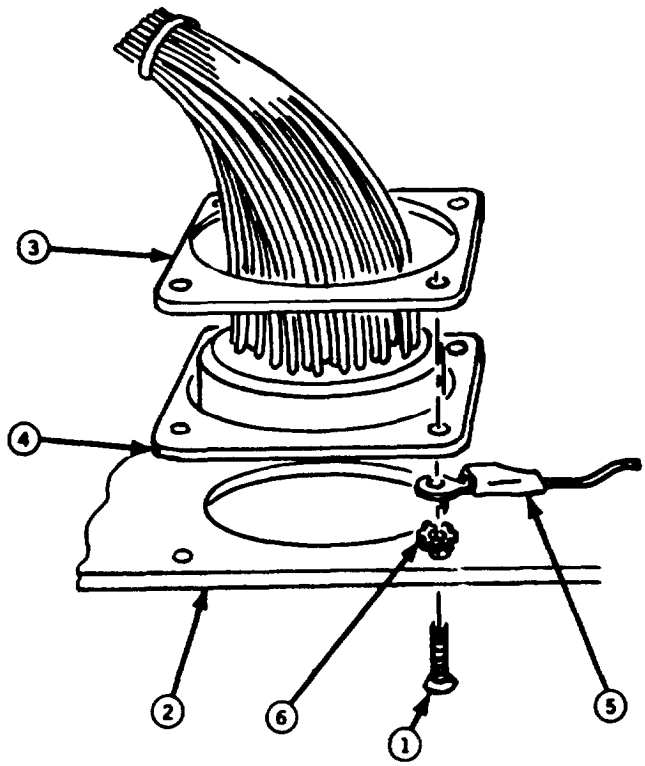
If more than one connector is being removed, tag each connector harness with its J number, as marked on front panel.

(1) Remove front panel (para 3-30).

(2) Remove four screws (1) from front panel (2).

(3) Remove plate (3) from back of connector (4).

(4) Remove connector (4), ground wire (5), and star washer (6) from front panel (2).



EL9JZ181

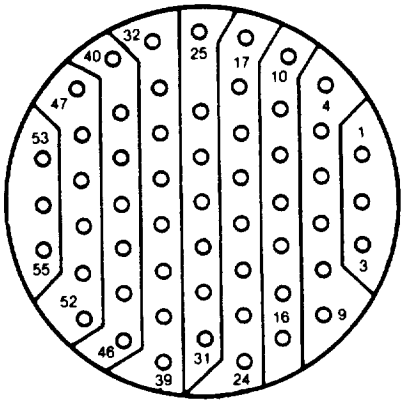
b. Repair.

NOTE

This procedure is for replacement of socket inserts on front panel connectors and is typical for replacement of socket inserts or pin inserts on the other connectors in the unit.

If more than one pin or socket insert is to be replaced, tag each wire.

(1) Locate socket insert to be replaced.



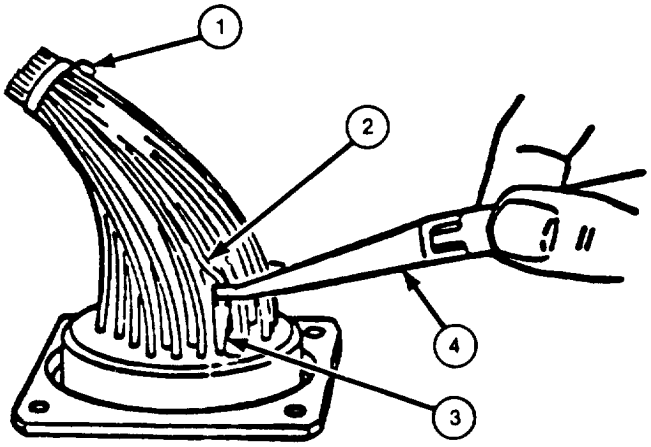
FRONT PANEL CONNECTOR
FRONT VIEW

CAUTION

When removing cable ties, use care not to cut wires.

(2) Cut cable ties (1) as needed to gain access to wires (2).

(3) Aline wire (2) of socket insert (3) to be removed with slotted part of removal tool (4).



EL8JZ182

NOTE

Removal tool will seat midway between the two bevels when removing a socket insert from a connector.

(4) Insert removal tool (4) into socket hole (5) to level of insertion shown.

NOTE

When removing socket insert, hold wire against removal tool, as shown.

(5) Press front part of removal tool (4) together to grasp socket insert (3). Hold wire (2) against tool (4) and lift out tool (4) with socket insert (3).

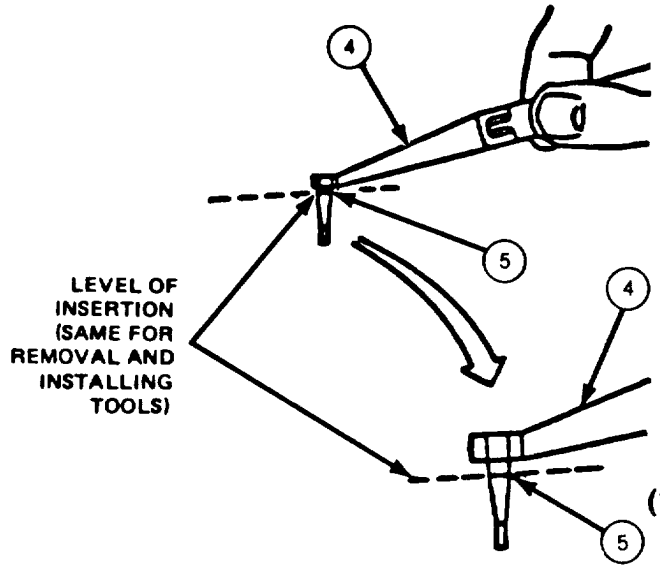
(6) Cut off damaged socket insert (3) as close to crimped end as possible.

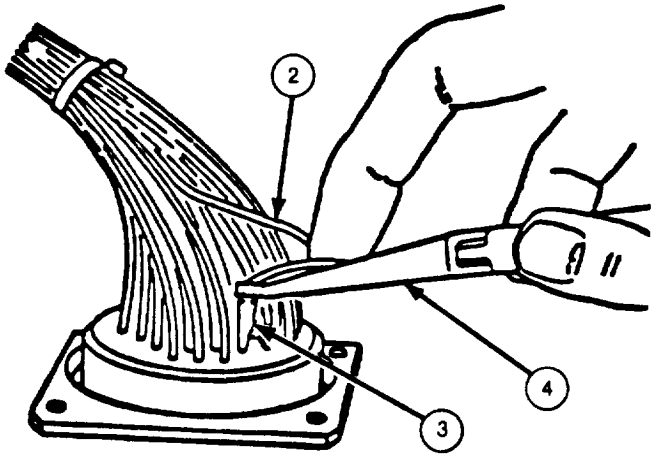
(7) Strip 3/32 to 1/8 inch of insulation from end of wire (2).

(8) Put replacement socket insert (3) on stripped end of wire (2).

(9) Crimp socket insert (3).

(10) Place wire (2) with attached socket insert (3) in tip of installing tool (4).





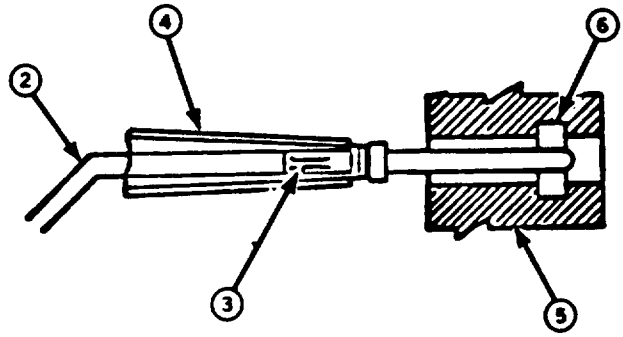
EL9JZ183

NOTE

The installing tool is inserted into connector to the same depth as removal tool.

(11) Install socket insert (3) into connector (5).

(12) Give wire (2) a slight pull to make sure socket insert (3) is locked in locking groove (6).



c. Replacement.

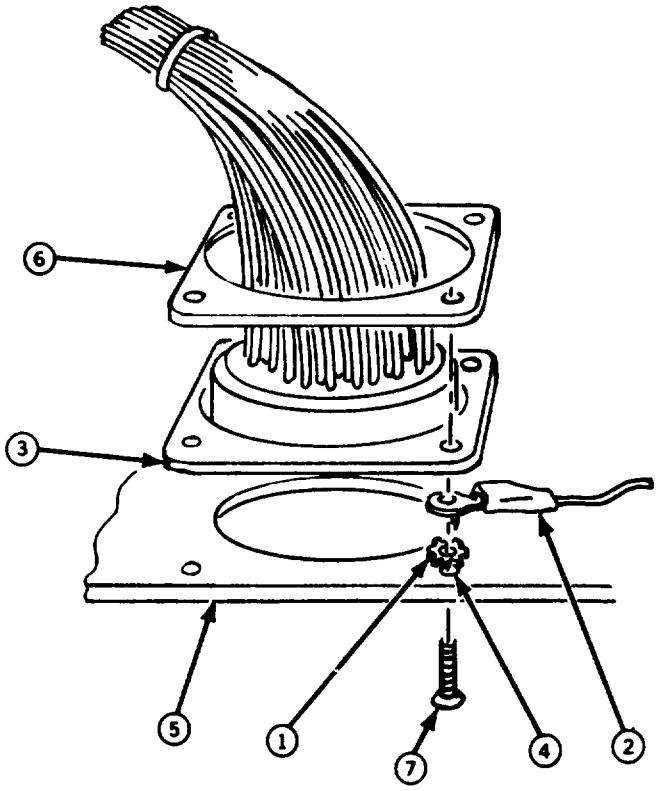
(1) Aline star washer (1), ground wire (2), and connector (3) with mounting holes (4) on front panel (5).

(2) Position plate (6) on back of connector (3).

(3) Install four screws (7) on front panel (5).

(4) Replace cable ties that were removed.

(5) Install front panel (para 3-30).



EL9JZ184

3-52. EMI FILTER CONNECTOR P30 REPAIR

This procedure is for the semiconductor and core memory processors.

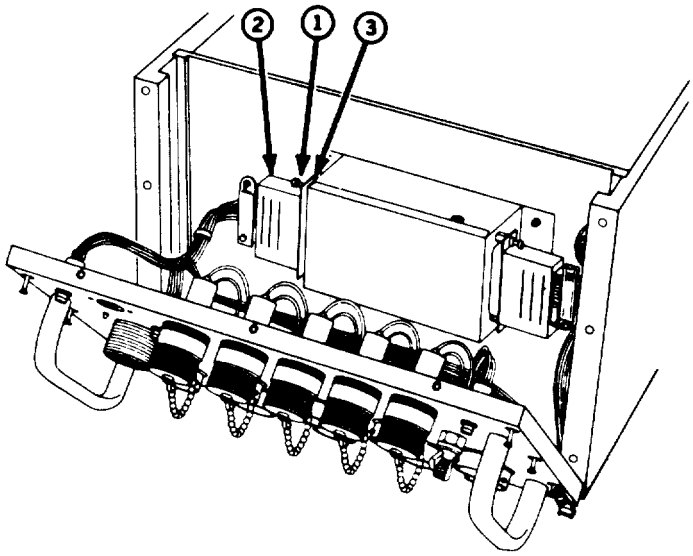
WARNING

Turn off power before working on equipment. Failure to do so can cause serious injury to personnel.

a. Removal.

(1) Remove front panel (para 3-30).

(2) Loosen two captive screws (1) and remove connector P30 (2) from EMI filter receptacle J30 (3).



b. **Repair**

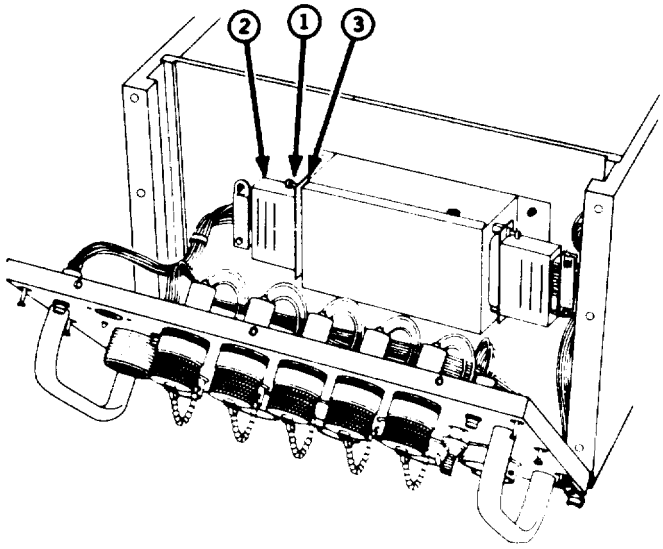
(1) Repair socket inserts (para 3-51).

c. Replacement.

(1) Position connector P30 (2) on EMI filter receptacle J30 (3).

(2) Tighten two captive screws (1).

(3) Install front panel (para 3-30).



EL9JZ185

3-53. POWER SUPPLY CONNECTOR J15 REPAIR

This procedure is for the semiconductor and core memory processors.

WARNING

Turn off power before working on equipment. Failure to do so can cause serious injury to personnel.

a. Removal.

(1) Remove power supply (para 3-34).

(2) Remove two screws (1), washers (2), and lockwashers (3) and remove connector J15 (4) from mounting bracket (5).

b. Repair.

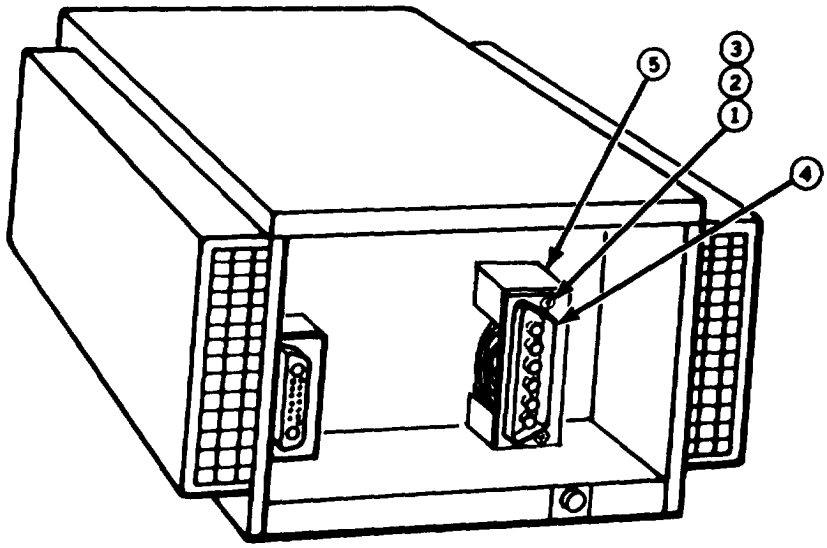
(1) Repair pin or socket inserts (para 3-51).

c. Replacement.

(1) Position connector J15 (4) on mounting bracket (5).

(2) Install two washers l-b8-2), lockwashers (3), and screws (1).

(3) Install power supply (para 3-34).



EL9JZ186

3-54. BLOWER FAN POWER PLUG P1 REPAIR

This procedure is for the semiconductor and core memory processors.

WARNING

Turn off power before working on equipment. Failure to do so can cause serious injury to personnel.

a. Removal.

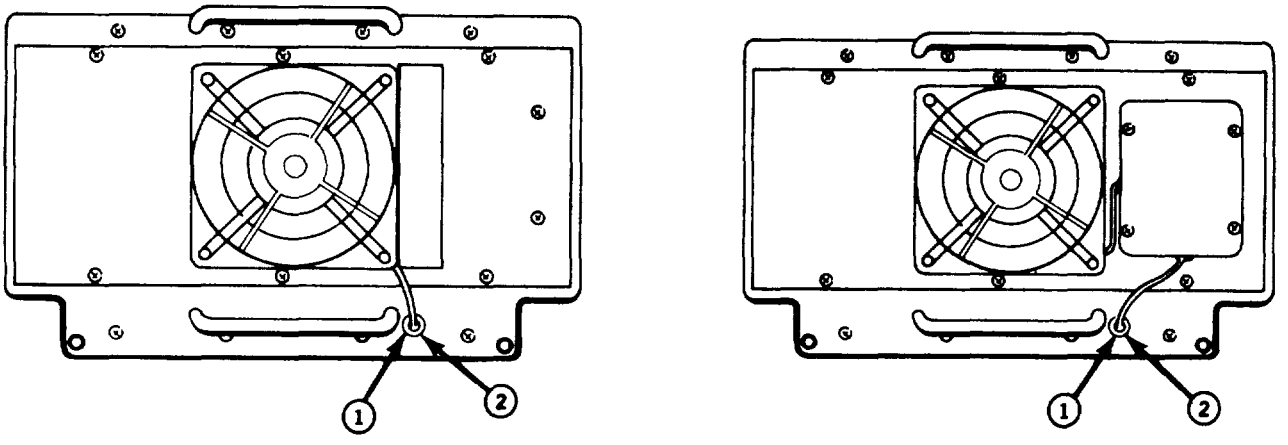
(1) Remove plug P1 (1) from connector J17 (2).

b. Repair

(1) Repair pins (para 3-51).

c. Replacement.

(1) Install plug P1 (1) on connector J17 (2).



EL9JZ187

3-55. BLOWER FAN POWER CONNECTOR J17 REPAIR

This procedure is for the semiconductor and core memory processors.

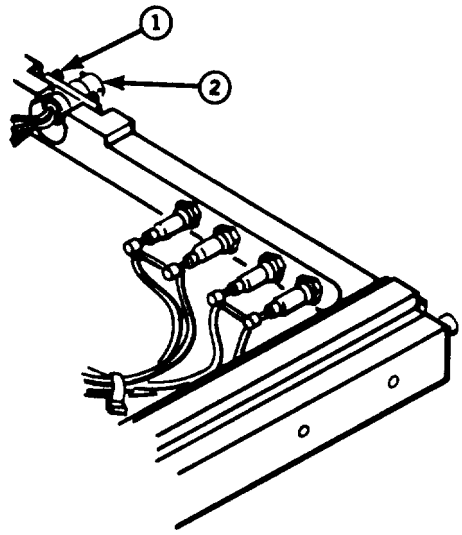
WARNING

Turn off power before working on equipment. Failure to do so can cause serious injury to personnel.

a. Removal.

(1) Remove power supply (para 3-34).

(2) Remove four screws (1) on connector (2). Remove connector (2).



b. Repair.

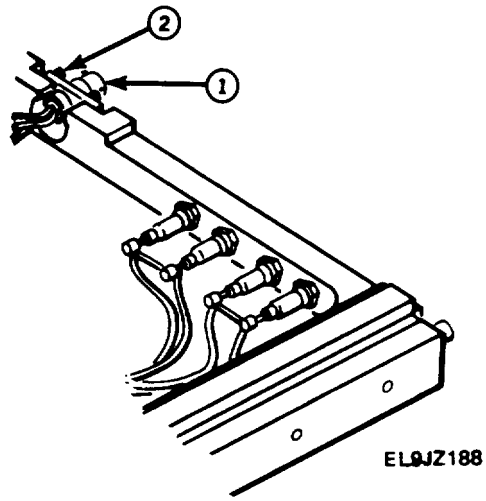
(1) Repair pin inserts (para 3-51).

c. Replacement.

(1) Position connector (1).

(2) Install four screws (2) on connector (1).

(3) Install power supply (para 3-34).



3-56. POWER INTERCONNECT HARNESS CONNECTOR P13 REPAIR

This procedure is for the semiconductor and core memory processors.

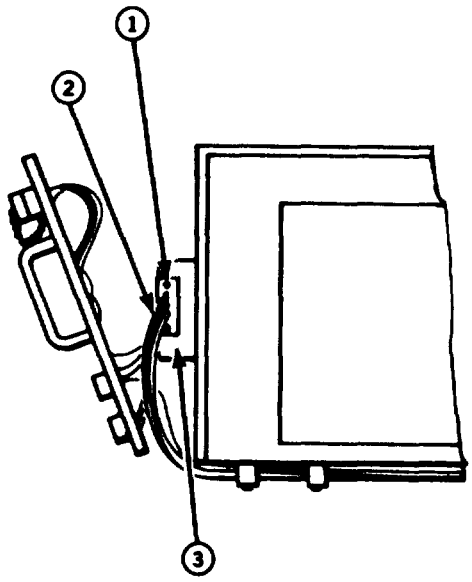
WARNING

Turn off power before working on equipment. Failure to do so can cause serious injury to personnel.

a. Removal.

(1) Remove front panel (para 3-30).

(2) Loosen two captive screws (1) and remove connector P13 (2) from EMI fiiter receptacle J31 (3).



EL9.JZ189

b. Repair.

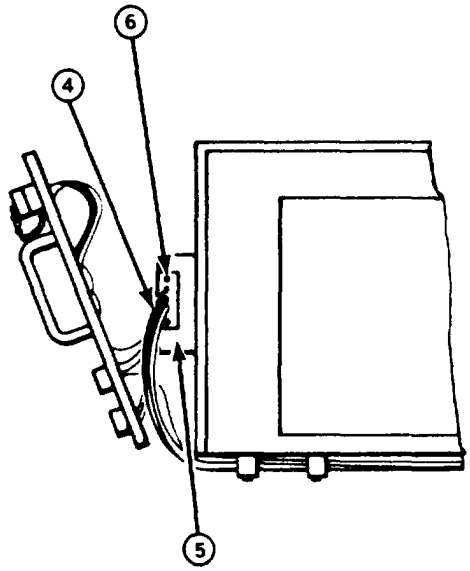
(1) Repair socket inserts (para 3-51).

c. Replacement.

(1) Position connector P13 (4) on EMI filter receptacle J31 (5).

(2) Tighten two captive screws (6).

(3) Install front panel (para 3-30).



EL9JZ191

3-57. POWER INTERCONNECT HARNESS CONNECTOR J14 REPAIR

This procedure is for the semiconductor and core memory processors.

WARNING

Turn off power before working on equipment. Failure to do so can cause serious injury to personnel.

a. Removal.

(1) Remove power supply (para 3-27).

(2) Remove top front cover plate (para 3-34).

(3) Remove bottom cover plate (para 3-28).

(4) Remove three screws (1) that attach top rear cover plate (2) to power supply bulkhead (3).

(5) Remove six screws (4) that attach top rear cover plate (2) to side panels (5). Remove top rear cover plate (2).

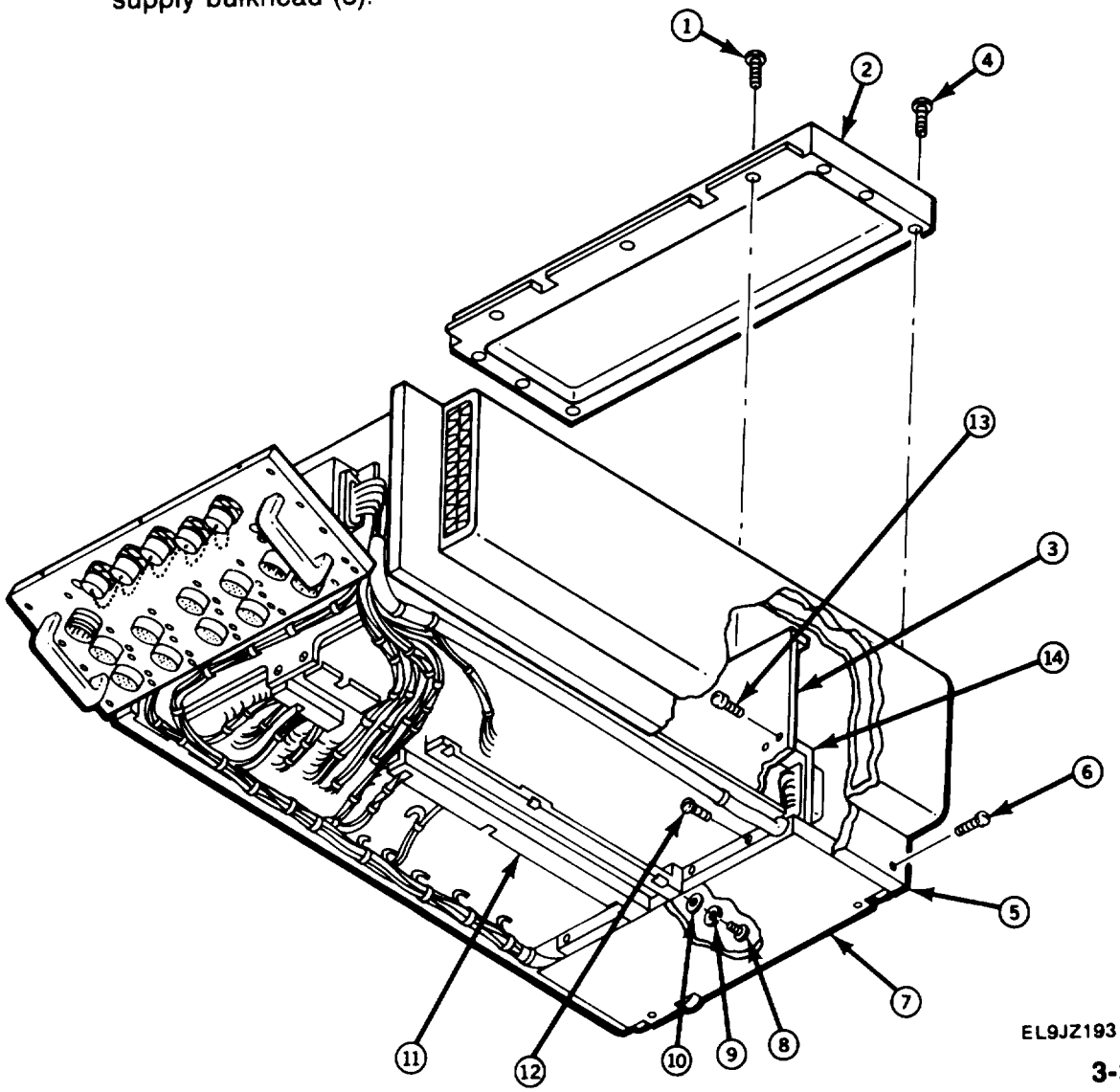
(6) Remove sixe screws (6) that attach bottom stiffener (7) to side panel (5).

(7) Remove two screws (8), lockwashers (9), and washers (10) that attach power supply bulkhead (3) and bottom stiffener (7) to motherboard stiffener (11).

(8) Remove four screws (12) from back side of bottom stiffener (7).

(9) Tilt power supply bulkhead (3) and bottom stiffener (7) forward.

(10) Remove four screws (13) for connector supports (14) from rear of power supply bulkhead (3).



EL9JZ193

b. Repair.

(1) Repair socket inserts (para 3-51).

c. Replacement.

(1) Position connector supports (1). Install four screws (2) for connector supports (1) from rear of power supply bulkhead (3).

(2) Position power supply bulkhead (3).

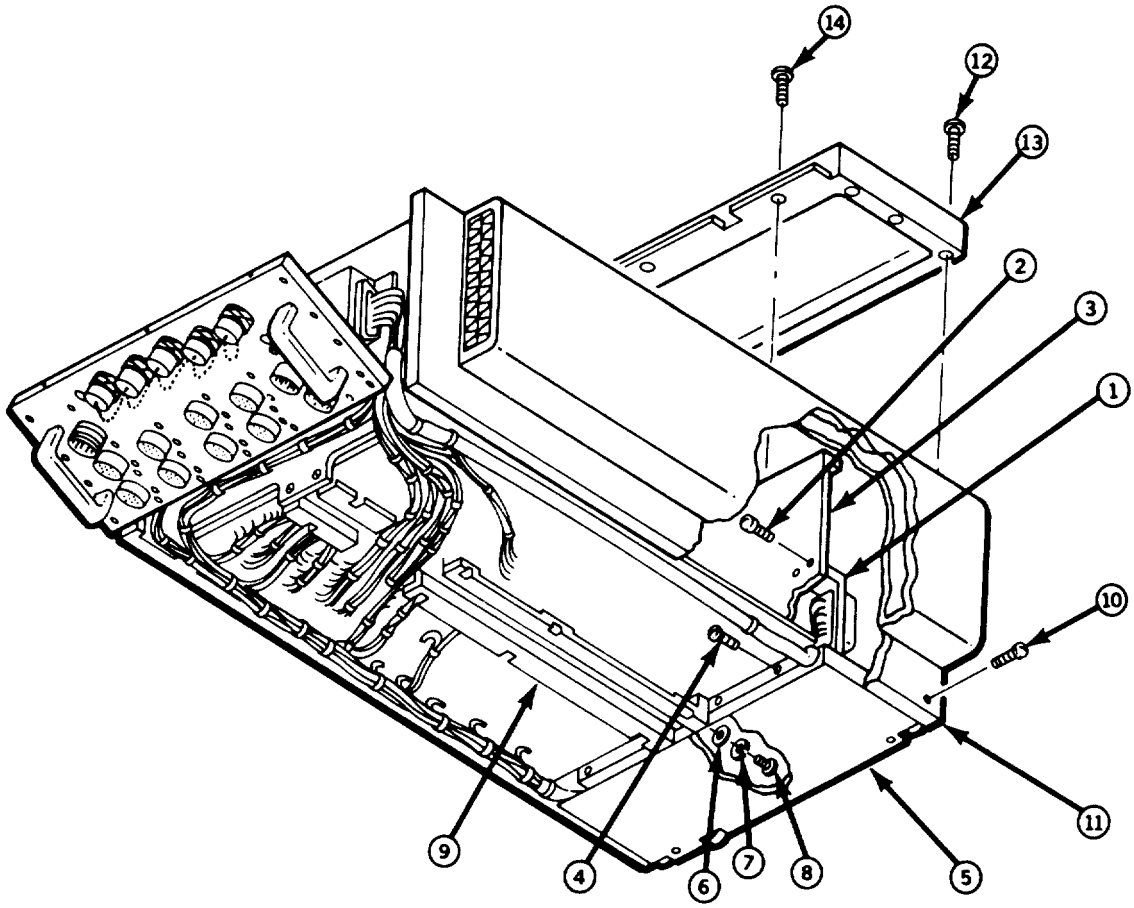
(3) Install four screws (4) on back side of bottom stiffener (5).

(4) Install two washers (6), lockwashers (7), and screws (8) that attach power supply bulkhead (3) and bottom stiffener (5) to motherboard stiffener (9).

(5) Install six screws (10) that attach bottom stiffener (5) to side panel (11).

(6) Install six screws (12) that attach top rear cover plate (13) to side panels (11).

(7) Install three screws (14) that attach top rear cover plate (13) to power supply bulkhead (3).



EL9JZ194

(8) Install bottom cover plate (para 3-28).

(9) Install power supply (para 3-34).

(10) Install top front cover plate (para 3-27).

3-58. CHASSIS REPAIR

If the processor chassis, or frame, is damaged, such as dents, cracks, or distortion, forward damaged unit to next higher level of maintenance.

CHAPTER 4

GENERAL SUPPORT MAINTENANCE INSTRUCTIONS

Section I. GENERAL INFORMATION

4-1. GENERAL

This chapter discusses the general support maintenance concepts and provides instructions for maintaining the Data Processing Set AN/UYK-64(V). Included in this chapter are troubleshooting instructions, troubleshooting flowcharts, and testing procedures (including maintenance diagnostic program information).

The processor is a sophisticated and complex piece of electronic equipment. Isolation of failures to the circuit component level usually requires the services of a throughly trained technician. However, the modular construction of the processor allows straightforward isolation of failures and easy replacement at the module level.

There are three basic approaches to maintenance planning; the optimum approach depends on the specific requirements of each application.

a. **Chassis Replacement.** In the event of a failure, an entire unit of equipment is replaced with a spare operational processor. This method minimizes mean-time-to-repair (MTTR), which can be a matter of seconds. The failed unit is then forwarded to the appropriate level of maintenance for repair. This approach is especially attractive for installations with several identical processors or installations having spare units.

b. **Module Replacement.** in the event of failure, the fault is localized and isolated to a replaceable module (assembly, subassembly, or major component), and a spare module is installed. MTTR with this method is usually less than an hour. This approach is economically preferable to unit replacement (para a above) in those installations with several processors of differing configurations. The failed module is forwarded to the appropriate level of maintenance for repair or replacement.

c. **Component Replacement.** in the event of failure, the fault is localized and isolated to the failed component, which is then replaced. This approach is not attempted except at general support maintenance, Special Repair Activity (SRA) facilities, or at depot maintenance. Refer to the Maintenance Allocation Chart (MAC) in TM 11-7021-202-12. Component replacement requires considerable technical skill, sparing of a Iarge number of component types, and can require hours of troubleshooting and repair time.

4-2. INSPECTIONS

The processor requires a minimum of periodic inspection and maintenance. Refer to the MAC and the preventive maintenance checks and service (PMCS) contained in TM 11-7021-202-12.

If the processor operates in a vibration environment (e.g., a moving vehicle), an occasional check of external screw tightness is performed. In particular, the screws holding the side rails on the printed circuit boards (PCBs) conductive heat path are tightened. A visual inspection of the system cables and connectors is also made prior to each deployment.

When the processor has not been operated for some time, it is checked out in an operational system configuration before use. Refer to paragraph 3-12.

Section II REPAIR PARTS, SPECIAL TOOLS, TMDE, AND SUPPORT EQUIPMENT

4-3. TOOLS AND TEST EQUIPMENT

Tools and test equipment required for general support maintenance of the equipment are listed in the Maintenance Allocation Chart (MAC) in TM 11-7021-202-12.

4-4. SPECIAL TOOLS, TMDE AND SUPPORT EQUIPMENT

Special tools, TMDE, and support equipment are listed and illustrated in the repair parts and special tools list (RPSTL) TM 11-7021-202-34P covering general support maintenance for this equipment.

4-5. REPAIR PARTS

Repair parts are listed and illustrated in the repair parts and special tools list (RPSTL) TM 11-7021-202-34P, covering general support maintenance for this equipment.

Section III. TROUBLESHOOTING

4-6. GENERAL

Refer to chapter 3, section III for troubleshooting instructions.

Section IV. TESTING PROCEDURES

4-7. GENERAL

Refer to chapter 3, section IV for testing procedures. Testing of the printed-circuit boards (PCBs) is not an activity of general support maintenance; refer to the Maintenance Allocation Chart (MAC) contained in appendix B of TM 11-7021-202-12 for maintenance responsibility guidance.

Section V. REMOVAL AND REPLACEMENT PROCEDURES

4-8. GENERAL

Refer to chapter 3, section V for removal and replacement instructions.

Section VI. REPAIR PROCEDURES

4-9. GENERAL

Refer to chapter 3, section VI for repair procedures. The repair of printed circuit boards (PCBs) and the processor's motherboard is not an activity of general support maintenance; refer to the Maintenance Allocation Chart (MAC) contained in appendix B of TM 11-7021-202-12 for maintenance responsibility guidance.

CHAPTER 5

PACKING FOR SHIPPING OR STORAGE

5-1. GENERAL

This chapter provides instructions for preparing the Data Processing Set AN/UYK-64(V) for shipping or storage. The processor chassis/mainframe, power supply, and printed circuit boards (PCBs) should be packaged and packed separately for shipment or storage. Material used for packaging and packing is listed in the expendable supplies and materials list (ESML) contained in appendix D. Instructions contained herein, reference each item in the ESML as it is used.

5-2. PREPARATION FOR STORAGE OR SHIPMENT

a. Prior to packaging and packing the processor and/or any of its subassemblies, perform the applicable routine PMCs. Refer to chapter 2 of TM 11-7021-202-12.

b. Clean the processor in accordance with chapter 3 of TM 11-7021-202-12.

c. Inspect the processor in accordance with chapter 3 of TM 11-7021-202-12.

d. The processor, its power supply and PCBS will, if possible, be repacked in their original packing containers.

e. Precautionary marking, special identification information, and shipping/handling instructions (as applicable) shall appear on all shipping/storage containers.

f. Administrative storage of the processor or its major components shall be in accordance with paragraph 1-4 of this manual.

5-3. EQUIPMENT DISASSEMBLY

Following are illustrated step-by-step procedures for removing certain components from the processor in anticipation of shipping and/or storage. As required, perform each procedure in the sequence they appear in this paragraph; e.g., paragraph a., then paragraph **b.,** then paragraph c., etc.

a. **Remove Power Cable.**

WARNING

Turn off power before working on equipment. Failure to do so can cause serious injury to personnel.

(1) If required, remove plug (1) from power source.

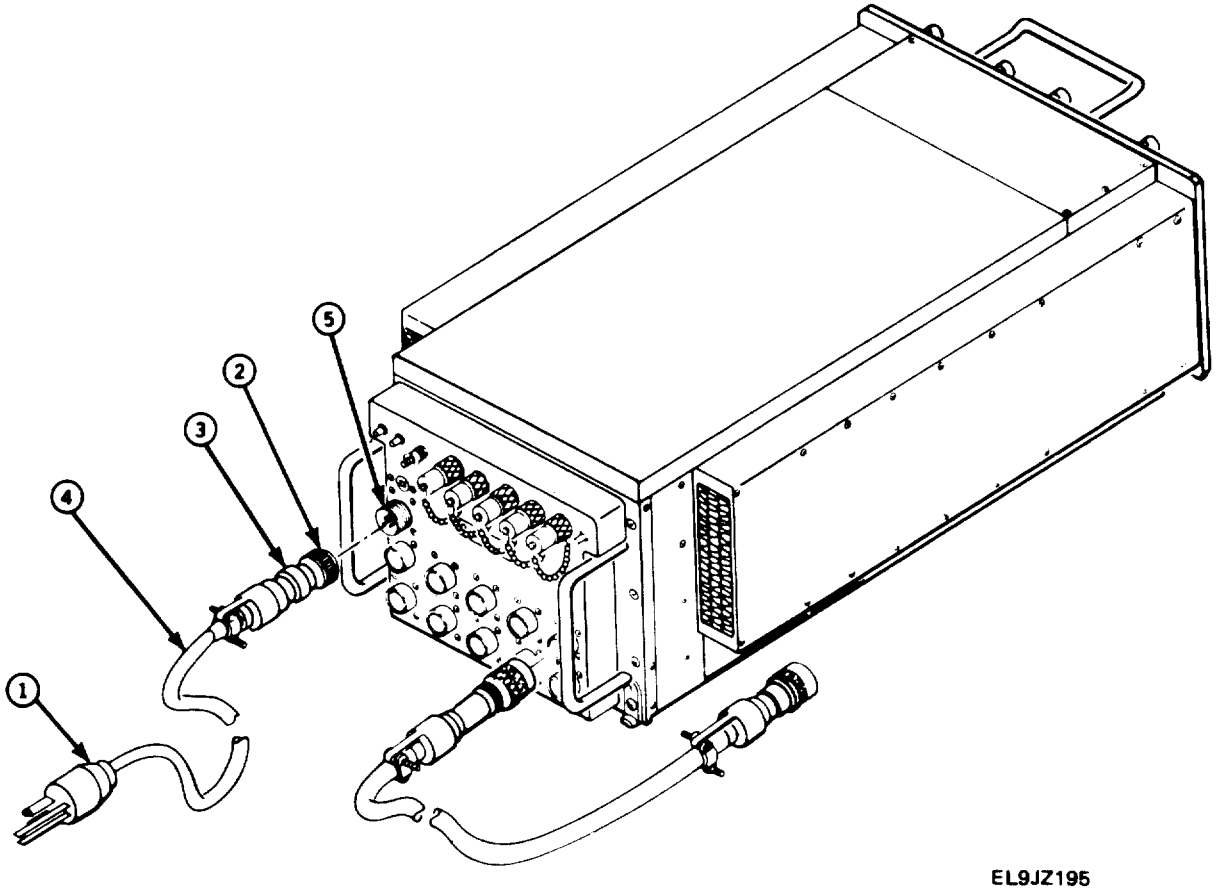
(2) Unscrew knurled nut (2) to left and unplug connector (3).

(3) Remove power cable (4).

(4) Place a dust cover on the now uncovered power input connector (5).

(5) Place dust cover on the connector (2) at end of the cable (4).

(6) Place the cable (4) in a clean plastic bag (item 15, appx B).



EL9JZ195

b. Remove I/O Cables.

(1) Turn knurled ring (1) to the left and unplug I/O cable connector (2) from processor connector (3).

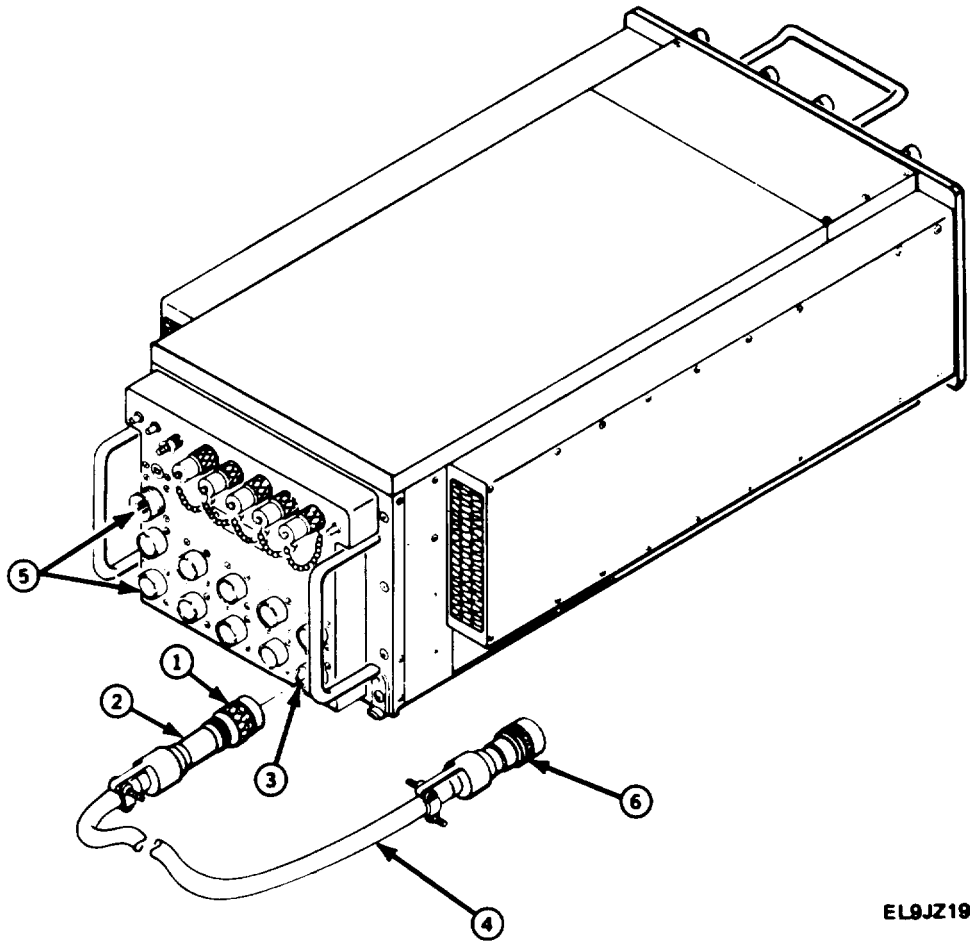
(2) Remove I/O cable (4).

(3) Repeat steps 1 and 2 to remove the balance of I/O cables connected to the processor.

(4) Place dust covers on all uncovered front panel connectors (5).

(5) Place dust covers on the connectors (1), (6) at each end of each I/O cable (4).

(6) Place each I/O cable (4) in a clean plastic bag (item 15, appx B).



c. Remove Top Cover Plate. Refer to paragraph 3-27.

d. Remove PCBs. Refer to paragraph 3-29.

e. Install Top Cover Plate. Refer to paragraph 3-27.

f. Remove Power Unit Assembly/Power Supply. Refer to paragraph 3-34. Place dust covers or protective covering over exposed rear unit connectors. Place dust covers or protective covering over the exposed power supply connectors.

5-4. PROCESSOR PACKAGING AND PACKING

When packaging and packing the processor for shipment or storage, see figure 5-1 and perform each of the following steps:

1. Install two desiccant bags (item 6, appx B) in a plastic bag (item 7, appx B).

WARNING

The processor is a heavy piece of equip ment. Always use two technicians when moving or lifting the unit to prevent injury to personnel.

2. Place the unit in the plastic bag (item 7, appx B).

3. Place all maintenance forms and tags in the plastic bag with the unit and seal the plastic bag with tape (item 8, appx B).

4. Place the bag containing the unit in a polyurethane foam container (item 9, appx B).

5. Place the polyurethane cover (item 11, appx B) on the container and seal with pressure sensitive tape (item 10, appx B).

6. Wrap the polyurethane container with a barrier material (item 12, appx B).

7. Secure the wrapping material with tape (item 8, appx B).

8. Complete shipping label (item 20, appx B) and affix it to the carton (item 13, appx B).

9. Complete shipping forms, place forms in packing list envelope (item 15, appx B), and affix the envelope to the carton.

5-5. POWER SUPPLY PACKAGING AND PACKING

Package the power supply indiviudally. Preparation and packaging shall be in accordance with paragraph 5-2.

When packaging a power supply (ac or dc) for shipment, refer to figure 5-1 and perform each of the following steps:

1. Install two desiccant bags (item 6, appx B) in a plastic bag (item 16, appx B).

2. Place the power supply in the plastic bag.

3. Place all maintenance forms and tags in the plastic bag with the power supply and seal the plastic bag with tape (item 8, appx B).

4. Place the bag containing the unit in a polyurethane foam container (item 19, appx B).

5. Place a polyurethane cover (item 17, appx B) on the container and seal with pressure sensitive tape (item 10, appx B).

6. Wrap the polyurethane container with a barrier material (item 12, appx B).

7. Secure the wrapping material with tape (item 8, appx B).

8. Place the barrier-wrapped package in a close fitting fiberboard box (item 18, appx B). Close the box and seal with reinforced tape (item 14, appx B).

9. Complete shipping label (item 20, appx B) and affix it to the carton.

10. Complete shipping forms, place forms in packing list envelope (item 15, appx B) and affix the envelope to the carton.

5-6. PRINTED CIRCUIT BOARD (PCB) PACKAGING AND PACKING

Each PCB is individually packaged in its own container before shipment. See figure 5-2 and perform each of the following steps:

1. Place the PCB on a sheet of cushioning material (item 21, appx B) that is at least twice the size of the PCB. Wrap the PCB in the cushioning material and secure with tape (item 8, appx B).

2. Place the wrapped PCB in a plastic bag (item 22, appx B).

3. Place all maintenance forms and tags in the plastic bag along with the PCB, then seal the bag with tape (item 8, appx B).

4. Place the plastic bag and PCB in shipping carton (item 23, appx B) and seal the carton with waterproof tape (item 10, appx B).

5. Complete shipping label (item 20, appx B) and affix it to the carton.

6. Complete shipping forms, place forms in packing list envelope (item 15, appx B), and affix the envelope to the carton as shown.

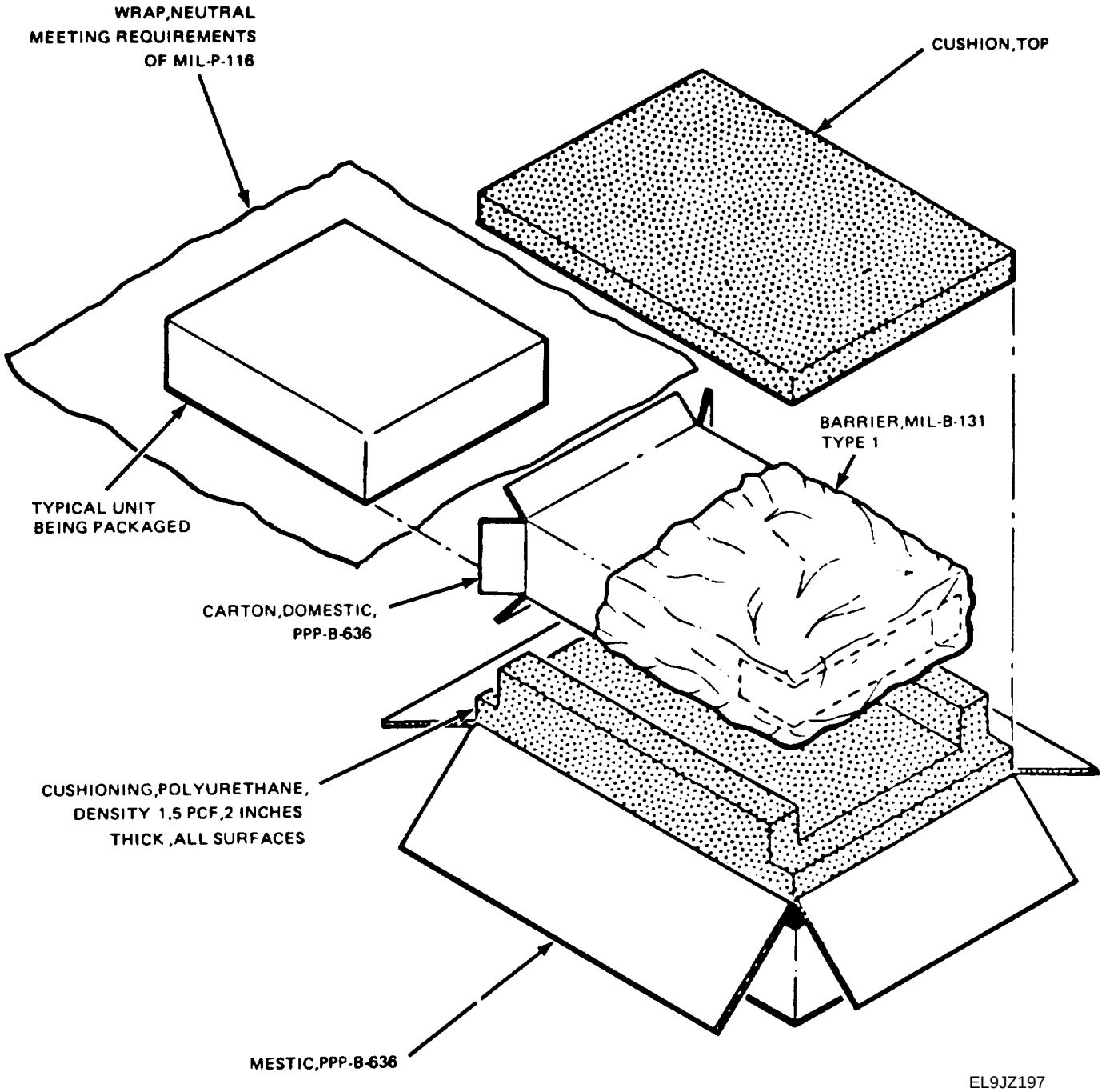


Figure 5-1. Packing a Typical Unit

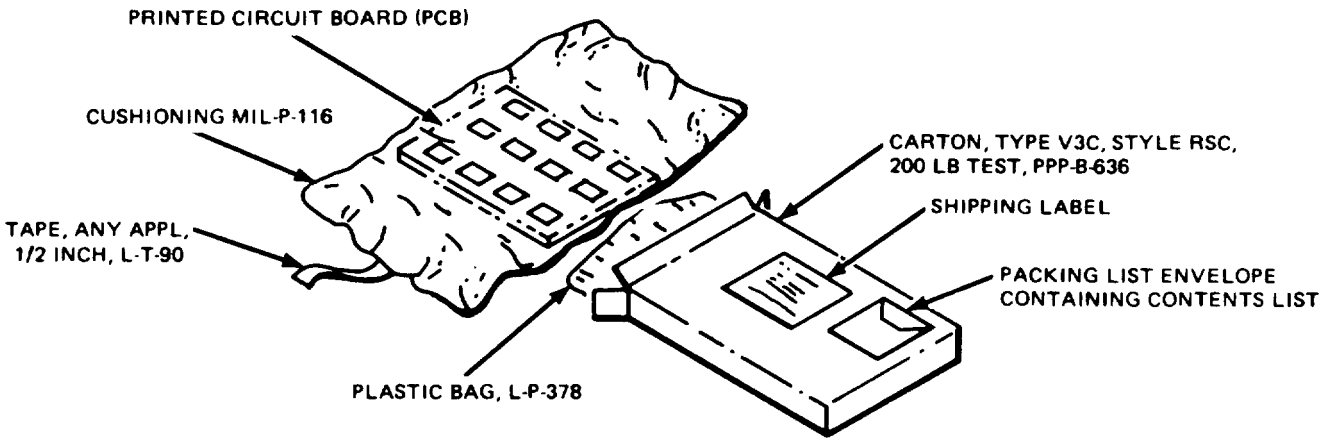


Figure 5-2. Packing a PCB

APPENDIX A

REFERENCES

A-1. SCOPE

This appendix lists all forms and technical publications referenced in this manual,

A-2. FORMS

Recommended Changes to Equipment Technical Manuals . . . . . DA Form 2028-2

Recommended Changes to Publications and Blank Forms . . . . . DA Form 2028

Equipment Inspection and Maintenance Work Sheets . . . . . DA Form 2404

Maintenance Request . . . .DA Form 2407

Equipment Log Assembly (Records).. . . . . DA Form 2408

Equipment Daily Log . . . . DA Form 2408-1

Equipment Modification Record . . . .DA Form 2408-5

Discrepancy in Shipment Report . . . .SF 361

Report of Discrepancy . . . .SF 364

Quality Deficiency Report . . . .SF 368

A-3. TECHNICAL BULLETINS

Solder and Soldering . . . . TB SIG 222

A-4. TECHNICAL MANUALS

Organizational Maintenance, Repair Parts and Special Tools List, Data Processing Set AN/UYK-64(V) . . . . . TM 11-7021-202-20P

Operator's and Organizational Maintenance Manual, AN/UYK-64(V) Data Processing Set . . . . TM 11-7021-202-12

Direct Support and General Support Maintenance Repair Parts and Special Tools List, AN/UYK-64(V) Data Processing Set . . . . . TM 11-7021-202-34P

A-4. TECHNICAL MANUALS-CONTINUED

Packaging of Material Preservation . . . . TM 38-230-1

Packaging of Material: Packing. . . . . .. TM 38-230-2

Administrative Storage of Equipment . . . . . TM 740-90-1

Procedures for Destruction of Electronics Materiel to Prevent Enemy Use (Electronics Command) . . . . . TM 750-244-2

DS and GS Quality Control: Inspection Criteria, Inspector's Inspection Criteria . . . . TM 750-245-4

A-5. SUPPLY BULLETINS

Preservation, Packaging, and Packing Materials, Supplies, and equipment Used By the Army . . . . SB 38-100

Common Table of Expendable items . . . . CTA 50-970

A-6. PAMPHLETS

Consolidated lndex of Army Publications and Blank Forms ... . DA PAM 310-1

The Army Maintenance Management System (TAMMS) . . . . DA PAM 738-750

A-7. ARMY REGULATIONS

Dictionary of United States Army Terms . . . . AR 310-25

Catalog of Abbreviations and Brevity Codes . . . . AR 310-50

Classification, Reclassification Maintenance, Insurance and Reporting of Maintenance Training Aircraft . . . . AR 700-42

Reporting of Transportation Discrepancies in Shipments . . . .AR 55-38

A-8. FEDERAL SPECIFICATIONS AND STANDARDS

Box, Wood, Nailed, and Locked Corners PPP-B-621

Box, Shipping, Fiberboard PPP-T-636

Tape, Gummed, Paper, Reinforced, and Plain, for Sealing and Servicing PPP-T-45

A-8. FEDERAL SPECIFICATIONS AND STANDARDS-CONTINUED

Tape, Packaging, Waterproof.. . . . . ..PPP-T-60

Strapping, Steel, and Seals.... . . . . QQ-S781

A-9. MILITARY SPECIFICATIONS

Corrosion Removing and Metal Conditioning Compound
(Phosphoric Acid Base) 31069 . . . .- . . . ..- MIL-C-10578

Calibration System Requirements MIL-C-45662

Electronic Equipment, Airborne, General
Specifications for MIL-E-5400

inspection Equipment, Acquisition, Maintenance,
and Disposition of... . . . .MIL-I-5607

Insulating Compound, Electrical (for Coating Printed
Circuit Assemblies) MIL-I-46058

Printed Wiring Boards MIL-l-55110

Preservation-Packaging, Methods of. MIL-P-5510

Packaging, Preformed, Straight Thread Tube Fitting Box,
Type 1, Hydraulic MIL-P-5510

Shock Tests, High-impact, Shipboard Machinery, Equipment and
Systems, Requirements for.... . . . . .. MIL-S-45743

Soldering, Manual Type, High Reliability, Electrical
and Electronic Equipment. MIL-S-45743

Vartnish, Moisture and Fungus Resistant (for Treatment of
Communications, Electronic and Associated Equipment MIL-V-173

A-10. MILITARY STANDARDS

Quality Assurance Terms and Definitions MIL-STD-109

Marking for Shipping and Storage MIL-STD-129

Printed Wiring for Electronic Equipment MIL-STD-275

Standard General Requirements for Electronic Equipment MIL-STD-454

Requirements for Repair and Modification of Printed
Wiring Assemblies MIL-STD-1569

A-11 MISCELLANEOUS

Reporting of Quality Deficiency Data . . . . **AMCR 702-7**

First Aid for Soldiers . . . . **FM 21-11**

APPENDIX B

EXPENDABLE SUPPLIES AND MATERIALS LIST

B-1. GENERAL

This appendix lists expendable supplies and materials needed to repair and sustain the AN/UYK-64(V) Data Processing Set. These items are authorized by CTA 50-970, Expendable Items (except Medical, Class V, Repair Parts, and Heraldic Items).

B-2. EXPLANATION OF COLUMNS

a. Column (1) — Item Number. This number is assigned to the entry in the listing and is referenced in the narrative instructions to identify the material; e.g., "Use detergent (Item 4, Appendix B)."

b. Column (2) — Level. This column identifies the level of maintenance that requires the listed item.

F = Direct Support
G = General Support

c. Column (3) — National Stock Number. This is the National Stock Number assigned to the item; use it to request or requisition the item.

d. Column (4) — Description. indicates the Federal item name and, if required, a description to identify the item. The last line for each item indicates the Federal Supply Code for Manufacturer (FSCM) in parenthesis followed by the part number.

e. Column (5) — Unit of Measure (MEAS). indicates the measure used in performing the actual maintenance function. This measure is expressed by a two-character, alphabetical abbreviation (e.g., Ea, In, Pc). If the unit of measure differs from the unit of issue, requisition the lowest unit of issue that will satisfy the requirements.

EXPENDABLE SUPPLIES AND MATERIALS LIST

(1) ITEM NO.	(2) LEVEL	(3) NATIONAL STOCK NUMBER	(4) DESCRIPTION PART NO. AND FSCM	UNIT OF MEAS.
1	F, G	6810-00-753-4493	Alcohol: Isopropyl (81 349) MlL-A-1 0428, Grade A	Oz
2	F, G	7920-00-356-4694	Brush: Bristle (81348)	Ea
3	F, G	8305-00-267-3015	Cloth: Cheesecloth Cotton: Lint-less (81 348) CCC-C-440, Type ll, Class 2.	Yd
4	F, G		Detergent: Mild: Liquid	Oz
5	F, G		Tubing: Heat Shrinkable	Pc
6	F, G		Dessicant Bags	Ea
7	F, G		Plastic Bags Chassis Size)	Ea
8	F, G		Tape: Adhesive	Ea
9	F, G		Container: Foam: Chassis Size	Ea
10	F, G		Tape: Adhesive: Waterproof	Ft
11	F, G		Cover: Foam: Chassis Size	Ea
12	F, G		Material: Barrier	Ft

EXPENDABLE SUPPLIES AND MATERIALS LIST — CONTINUED

(1) ITEM NO.	(2) LEVEL	(3) NATIONAL STOCK NUMBER	(4) DESCRIPTION PART NO. AND FSCM	UNIT OF MEAS.
13	F, G		Box: Fibreboard: Chassis Size	Ea
14	F, G		Tape: Reinforced	Ft
15	F, G		Bag: Plastic: Forms and Tags	Ea
16	F, G		Bag: Plastic: Power Supply Size	Ea
17	F, G		Cover: Foam: Power Supply Size	Ea
18	F, G		Box: Fibreboard: Power Supply Size	Ea
19	F, G		Container: Foam: Power Supply Size	Ea
20	F, G		Label: Shipping	Ea
21	F, G		Paste, Thermal	Ea

APPENDIX C

SYSTEM CONFIGURATION DATA

C-1 GENERAL

Appendices C1 and C2 provide data on configuring the AN/UYK64(V) processor for use in various system configurations. Included in each appendix is a list of circuit cards used in the applicable configuration together with an illustration showing the location of each card.

C-2 HOW TO USE THIS APPENDIX

The following paragraphs provide instructions to configure a processor for use in a given system application.

a. Configuring the Processor

(1) Determine the system in which processor is to be used.

(2) Go to the appendix applicable to that system.

(3) The circuit card complement required for that system is listed in the appendix.

(4) Install the circuit cards into the processor in accordance with the PCB replacement instruction provided in Chapter 3.

(5) After configuring the processor, use the diagnostic test to verify proper operation.

b. Alternate Circuit Card Device Codes

When required, circuit cards are equipped with jumpers for standard device codes. To charge device codes on applicable circuit cards, go to the appendix applicable to that system. Using the information provided in the table and illustration in the appendix, remove or add jumpers as required for that system.

C-3 LIST OF SYSTEMS

The following is a list of systems that are covered in this appendix.

Systems	Appendix
AN/TSQ-114B Trailblazer	**C1**
AN/ASN -132 Inertial Navigation System	**C2**

APPENDIX C1

AN/TSQ-114B TRAILBLAZER

C1-1 GENERAL

This appendix contains data on how to configure the AN/UYK-64(V)1 for use in the AN/TSQ-1146 Trailblazer system. Refer to appendix D for configuration of AN/TSQ-1146 Trailblazer I/O chassis.

C1-2 SYSTEM CONFIGURATION DATA

Table C1-1 provides a list of circuit cards that will be installed in the AN/UYK-64(V)1 processor for the AN/TSQ-114B configuration. Figure C1-1 illustrates the circuit card complement for the AN/TSQ-114B.

C1-3 ALTERNATE DEVICE CODES

No alternate device codes are used for the AN/TSQ-114B Trailblazer system.

Table C1-1. Processor Circuit Cards

SLOT	CARD TYPE	DESCRIPTION	I/O CONNECTOR
A1	3561B	I/O BUS EXPANDER	J2
A2	3566	PRIORITY/LOAD MODULE	J3
A3	3566	PRIORITY/LOAD MODULE	J4
A4	3566	PRIORITY/LOAD MODULE	J5
A5	3566	PRIORITY/LOAD MODULE	J7
A6	3543	DIFFERENTIAL I/O BUFFER	J8
A7	3543	DIFFERENTIAL I/O BUFFER	J9
A8	4055	DISK DRIVE ADAPTER	J10
A9-A12	5711	CENTRAL PROCESSING UNIT	J11
A13-A15	1751	FLOATING POINT UNIT	
A16	1754	ERCC	
A17	1753	MEMORY CONTROL	
A18-A19	2030	64K WORD ARRAY	
A20	1753	MEMORY CONTROL	
A21-A22	2030	64K WORD ARRAY	
A23	5617	POWER SUPPLY (AC)	
A24	3883	EMI FILTER	

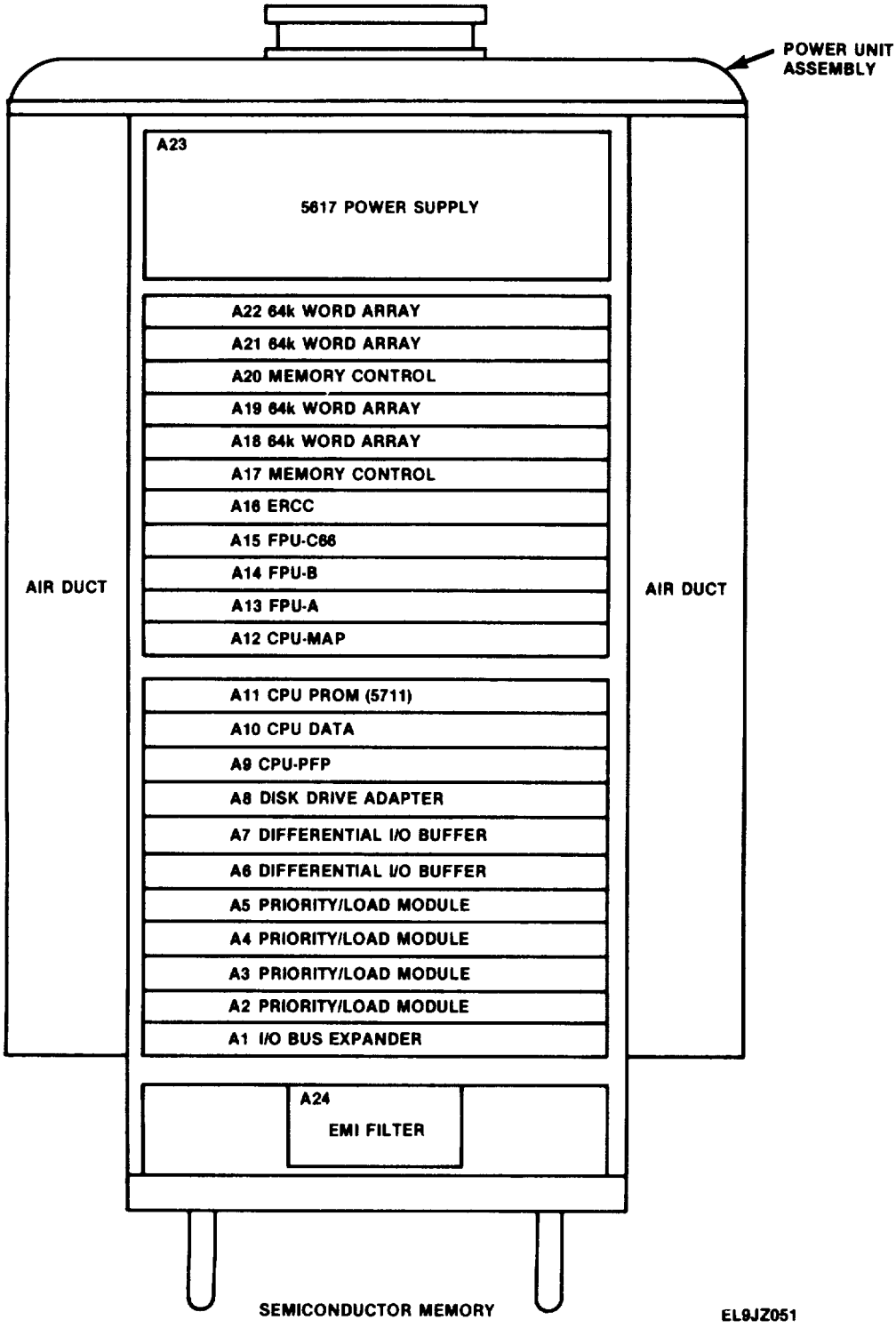


Figure C1-1. Processor Configuration for AN/TSQ-114B Trailblazer System

APPENDIX C2

AN/ASN-132 INERTIAL NAVIGATION SYSTEM

C2-1 GENERAL

This appendix contains data on how to configure the AN/UYK-64(V)2 for use in the AN/ASN-132 Inertial Navigation System.

C2-2 SYSTEM CONFIGURATION DATA

Table C2-1 provides a list of circuit cards that will be installed in the AN/UYK-64(V)2 processor for the AN/ASN-132 configuration. Figure C2-1 illustrates the circuit card complement for the AN/ASN-132

C2-3 ALTERATE DEVICE CODES

No alternate device codes are used for the AN/ASN-132 Inertial Navigation System.

Table C2-1. Processor Circuit Cards

SLOT	CARD TYPE	DESCRIPTION	I/O CONNECTOR
A1	3561B	I/O BUS EXPANDER	J2
A2	3566	PRIORITY/LOAD MODULE	J3
A3	3566	PRIORITY/LOAD MODULE	J4
A4	3566	PRIORITY/LOAD MODULE	J5
A5	3566	PRIORITY/LOAD MODULE	J7
A6	3566	PRiORITY/LOAD MODULE	J8
A7	3566	PRIORITY/LOAD MODULE	J9
A8	3761	SERIAL AIRCRAFT DATA BUS	J10
A9-A12	5711	CENTRAL PROCESSING UNIT	J11
A13-A15	1751	FLOATING POINT UNIT	
A16	1755	IMC/RMC	
A17-A19	2019	CORE MEMORY SET	
A20-A22	2019	CORE MEMORY SET	
A23	5617	POWER SUPPLY	
A24	3883	EM I FILTER	

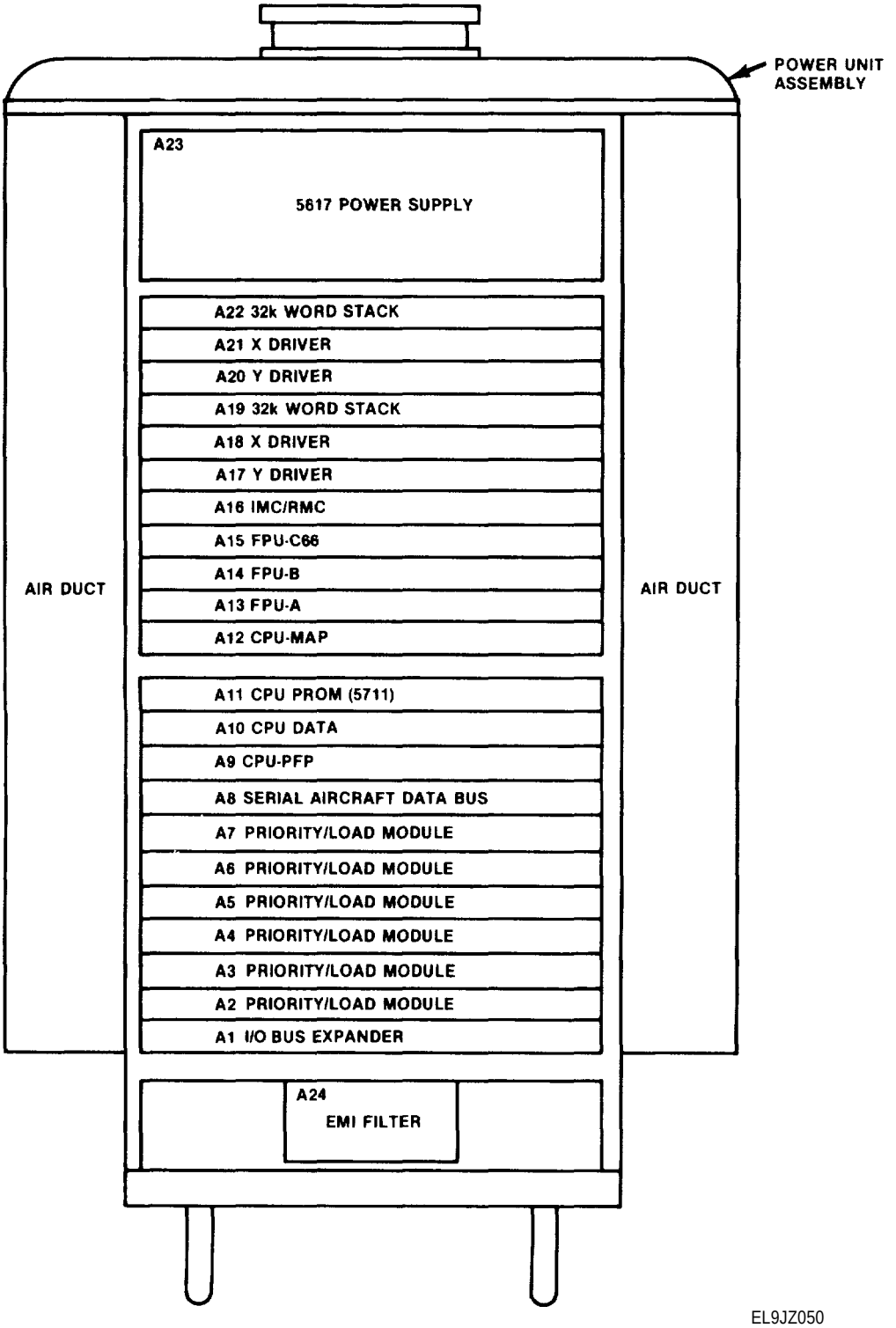


Figure C2-1. Processor Configuration for AN/ASN-132 Inertial Navigation System

APPENDIX D

SYSTEM I/O CONFIGURATION DATA

D-1 GENERAL

Appendix D1 provides data on configuring the I/O chassis for use in various system configurations. Included in each appendix is a list of circuit cards used in the applicable configuration together with an illustration showing the location of each card.

D-3 HOW TO USE THIS APPENDIX

The following paragraph provide instructions to configure an I/O chassis for use in a given system application.

a. Configuring the I/O Chassis

(1) Determine the system in which the I/O chassis is to be used

(2) Go to the appendix applicable to that system.

(3) The circuit card compement for that I/O chassis is listed in the appendix.

(4) Install the circuit cards in the I/O chassis in accordance with the PCB replacement instructions provided in Chapter 3.

(5) After configuring the I/O chassis, use the diagnostic test to verify proper operation.

b. Alternate Circuit Device Codes

When required, circuit cards are equipped with jumpers for standard device codes. To charge device codes on applicable circuit cards, go to the appendix applicable to that system. Using the information provided, remove or add jumpers required for that system.

D-3 LIST OF SYSTEMS

The following is a list of systems (configurations) that are covered in this appendix.

System	Appendix
AN/TSQ-l14B Trailblazer	D 1

APPENDIX D1

AN/TSQ-114B TRAILBLAZER I/O CHASSIS

D1-1 GENERAL

This appendix contains data on the configuration of the AN, TSQ-1146 Trailblazer I/O chassis. Refer to appendix C for the configuration of the AN/UYK-64(V)1 main processor.

D1-2 SYSTEM CONFIGURATION DATA

Table D1-1 provides a list of circuit cards that will be installed in the AN/TSQ-1146 Trailblazer I/O chassis. Figure D1-1 illustrates the circuit card complement for the AN/SQ-1146 Trailblazer I/O chassis.

D1-3 ALTERNATE DEVICE CODES

No alternate device codes are used for the AN/TSQ-1146 Trailblazer I/O chassis.

Table D1-1. I/O Chassis Circuit Cards

SLOT	CARD TYPE	DESCRIPTION	I/O CONNECTOR
A1	3566	PRIORITY/LOAD MODULE	J5
A2	3566	PRIORITY/LOAD MODULE	J10
A3	3566	PRIORITY/LOAD MODULE	J1
A4	3566	PRIORITY/LOAD MODULE	J6
A5	S667	CURRENT DRIVER	J2
A6	3566	PRIORITY/LOAD MODULE	J11
A7	S667	CURRENT DRIVER	J7
A8	S667	CURRENT DRIVER	J12
A10	S667	CURRENT DRIVER	J3
A11	3549	SYSTEM INTERRUPTS	J8
A12	3549	SYSTEM INTERRUPTS	J15
A13	3549	SYSTEM INTERRUPTS	J13
A14	3543	DIFFERENTIAL I/O BUFFER	J4
A15	3543	DIFFERENTIAL I/O BUFFER	J16
A16	3563	I/O BUS REPEATER	
A17	5616	POWER SUPPLY (AC)	J14
A18	3881	EMI FILTER	

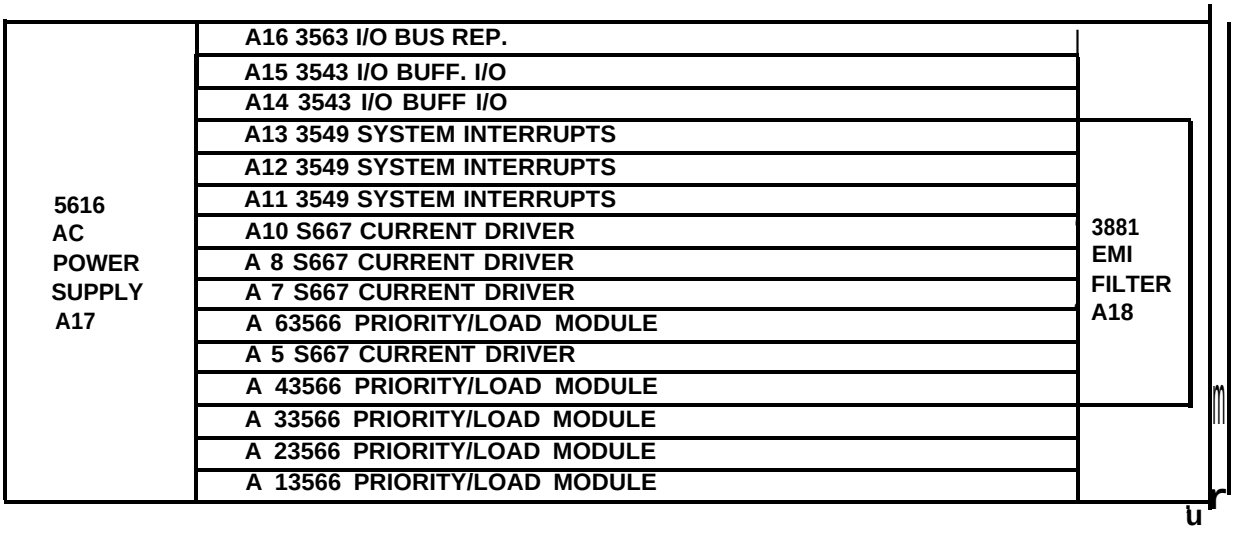


Figure D1-1. I/O Chassis Configuration for AN/TSQ-114B Trailblazer System

APPENDIX E

MX-10374/UYK and MX-10375/UYK I/O CONFIGURATION DATA

E-1 GENERAL

This appendix contains data on the configuration of the MX-10374/UYK and MX-10375/UYK I/O chassis. Both of these chassis are basic chassis that provide expansion capability for the AN/UYK-64(V) processor, as required for a given system application. No circuit card assemblies are provided with the MX- 10374UYK or the MX-10375/UYK chassis.

E-2 SYSTEM CONFIGURATION

Table E-1 provides a list of the circuit cards and modules contained in the MX-10374/UYK (ac) and the MX-10375/UYK (de) configurations. Figure E-1 illustrates the circuit card/module complement for the MX-10374/UYK and the MX-10375/UYK I/O chassis.

E-3 ALTERNATE DEVICE CODES

No alternate device codes are used for the MX-10374/UYK or the MX-10375/UYK I/O chassis.

Table E-1. I/O Chassis Circuit Cards/Modules

SLOT	CARD TYPE	DESCRIPTION	I/O CONNECTOR
A1-A16		BLANK	J14
A17	5616 (ac) or 5686 (de)	POWER SUPPLY	
A18	3881 (ac) or 3882 (de)	EMI FILTER	

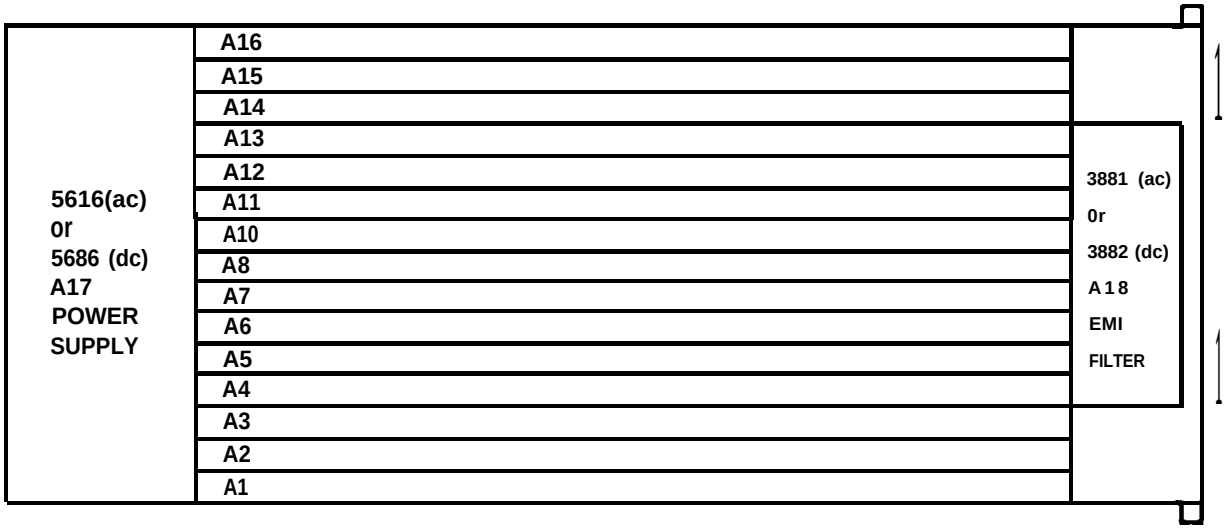


Figure E-1. MX-10374/UYK and MX-10375/UYK Configuration

APPENDIX F

TORQUE LIMITS

F-1. GENERAL

When replacing components, screws should be tightened to specific torque settings. Table F-1 provides these torque settings.

Table F-1. Torque Data

Component	No. of Screws	Torque (in-lbs.)
Top Front Cover Plate	16	7
Top Rear Cover Plate	6	7
Bottom Cover Plate	28	7
Air Duct	14(#4-40 X 1.63) 4(#6-32 X 1.63)	5 8
Blower Fan	45.2	
Power Unit Assembly	6	5
Power Supply	8	25
EMI Filter	4	3.5
Connectors J1 thru 11	4	7
Connectors J14 and J15	2	5
Connector J17	4	1.5
Connectors P30 and P31 (Semiconductor)	2	1.5
Connectors P12 and P13 (Core)	2	1.5

APPENDIX G

PROCESSOR WIRE LISTS AND MOTHERBOARD CONNECTIONS

G-1. SCOPE

This appendix contains wiring information for the interconnection of the semiconductor and core memory processor's components. This information is presented in the following tables.

- Table G-1. Front Panel Wire List (Semiconductor Processor)
- Table G-2. Front Panel Wire List (Core Memory Processor)
- Table G-3. Motherboard Wire List (Semiconductor Processor)
- Table G-4. Motherboard Wire List (Core Memory Processor)
- Table G-5. AC Power Supply Assembly Model 5617 Wire List
- Table G-6. DC Power Supply Assembly Model 5687 Wire List
- Table G-7. AC Power Unit Assembly Wire List

Table G-1. Front Panel Wire List (Semiconductor Processor)

FROM	TO	FUNCTION	COLOR
J1-A	F5-1	+28VDC RET	BLK
-B	F2-1	AC PHASE B	YEL
- c	F3-1	AC PHASE C	BLU
-D	F4-1	+ 28VDC	WHT
-E	F1-1	AC PHASE A	RED
J1-G	GND STUD	CHASSIS GND	GRN
GND STUD	P30-6	CHASSIS GND	GRN
GND STUD	P30-13	CHASSIS GND	GRN
F1-2	P30-3	AC PHASE A	RED
-2	P3O-10	AC PHASE A	RED
F2-2	P30-4	AC PHASE B	YEL
-2	P30-11	AC PHASE B	YEL
F3-2	P30-5	AC PHASE C	BLU
-2	P30-12	AC PHASE C	BLU
F4-2	P30-A1	+ 28VDC	WHT
F5-2	P30-A2	+ 28VDC RET	BLK
F12-1			

Table G-2. Front Panel Wire List (Core Memory Processor)

FROM	TO	FUNCTION	COLOR
J1-A	F5-1	+ 28VDC RET	BLK
-B	F2-1	AC PHASE B	YEL
-C	F3-1	AC PHASE C	BLU
-D	F4-1	+ 28VDC	WHT
-E	F1-1	AC PHASE A	RED
J1-G	GND STUD	CHASSIS GND	GRN
GND STUD	P12-6	CHASSIS GND	GRN
GND STUD	P12-13	CHASSIS GND	GRN
F1-2	P12-3	AC PHASE A	RED
-2	P12-10	AC PHASE A	RED
F2-2	P12-4	AC PHASE B	YEL
-2	P12-11	AC PHASE B	YEL
F3-2	F12-5	AC PHASE C	BLU
-2	P12-12	AC PHASE C	BLU
F4-2	P12-A1	+ 28VDC	WHT
F5-2	P12-A2	+ 28VDC RET	BLK

Table G-3. Motherboard Wire List (Semiconductor Processor)

FROM	TO	FUNCTION	COLOR
J11-1	E40	GND	BLK
-2	E37-1	-12V	BRN
-3	NC		
-4	E38-2	CTSIN	RED
-5	NC		
-6	E38-4	TTIN	YEL
-7	NC		
-8	NC		
-9	NC		
-10	E38-8	RDRRUN	GRA
-11	E38-3	EXTCLK	ORN
-12	NC		
-13	E60	GND	BLK
-14	E60	GND	BLK
-15	NC		
-16	NC		
-17	E38-1	CTSOUT	BRN
-18	NC		
-19	E38-5	TTOUT	GRN
-20	E37-2	+V12	RED
-21	NC		
-22	NC		
-23	NC		
-24	NC		
-25	S2-3	PRST*	ORN
-26	S2-1	GND	BLK
-27	NC		
-28	M1(*)	+ 5V	RED
J11-29	NC		
J11-30	S3-3	CONPL*	ORN
-31	S3-1	GND	BLK
-32	E38-6	CON LOCK*	BLU
-33	E60	GND	BLK
-34	NC		
-35	NC		
-36	NC		
-37	NC		
-38	NC		
-39	S2-4	RUN LITE	YEL
-40	S3-4	BITE*	WHT/YEL
J11-41	E19A	+5UP	RED

Table G.3. Motherboard Wire List (Semiconductor Processor)

FROM	TO	FUNCTION	COLOR
J11-42	NC		
-43	NC		
-44	NC		
-45	NC		
-46	NC		
-47	NC		
-48	NC		
-49	NC		
-50	NC		
-51	NC		
-52	NC		
-53	NC		
-54	NC		
J11-55	CHASSIS	CHASSIS GND	BLK
J6-A	J15-13	+BATT IN	WHT/ORN
-B	J15-14	+BATT IN	WHT/YEL
J6-C	NC		
J6-D	NC		
-E	J15-7	BATT RET	VIO
-F	J 15-8	BATT RET	GRA
-G	NC		
J6-H	J15-1	BATT CHARGE	BRN
J15-1	J6-H	BATT CHARGE	BRN
-2	E36	SMOK*	RED
-3	NC		
-4	NC		
-5	E25	-12V	GRN
-6	E25A	-12V	BLU
-7	J6-E	BATT RET	VIO
-8	J6-F	BATT RET	GRA
-9	E24	+12V	WHITE
-10	E24A	+12V	WHT/BLK
-11	E9	+5VSNS RET	WHT/BRN
-12	E10	+ 5V SNS	WHT/RED
-13	J6-A	+BATT IN	WHT/ORN
-14	J6-B	+BATT IN	WHT/YEL
-15	E39-8	+5 OK	WHT/GRN
-16	E41	MOK	WHT/BLU
-17	E39-7	PWR FAIL*	WHT/VIO
-A1	E2A	AUX V. RET	BLK
J15-A1	E4	AUX V. RET	BLK

Table G-3. Motherboard Wire List (Semiconductor Processor)

FROM	TO	FUNCTION	COLOR
J 15-A2	E22	+5 RET	BLK
-A2	E20	+5 RET	BLK
-A2	E18	+5 RET	BLK
-A2	E16	+5 RET	BLK
-A3	E14	+ 5 RET	BLK
-A3	E12	+ 5 RET	BLK
-A3	E8	+ 5 RET	BLK
-A3	E6	+ 5 RET	BLK
-A4	E1A	+ 5 VOLTS	WHT
-A4	E3	+ 5 VOLTS	WHT
-A4	E5	+ 5 VOLTS	WHT
-A4	E7	+ 5 VOLTS	WHT
-A5	E11	+ 5 VOLTS	WHT
-A5	E13	+ 5 VOLTS	WHT
-A5	E15	+ 5 VOLTS	WHT
-A5	E17	+ 5 VOLTS	WHT
-A7	E19	+5V MEM	GRA
J15-A7	E21	+5V MEM	GRA
E60	E39-4	GND	BLK
E60	E23-1	GND	BLK
S1-4	E60	GND	BLK
-2	E23-2	+ 5V	RED
S2-3	E39-3	PRST*	ORN
-1	E60	GND	BLK
-2	E39-5	+ 5V	RED
-4	A12J1-C9	RUN LITE	WHT
S3-2	E39-2	+ 5V	RED
-4	E39-1	BITE*	BRN
S3-1	E60	GND	BLK
S3-3	E38-7	CONPL*	ORN
DS1-1	E19A	+5V UP	RED
-2	E60	GND	BLK
M1(+)	E1	+ 5V	RED
M1(–)	E2	GND	BLK
P31-3	J 14-3	AC PHASE A	RED
-10	J14-10	AC PHASE A	RED
-4	J14-4	AC PHASE B	YEL
-11	J14-11	AC PHASE B	YEL
-5	J14-5	AC PHASE C	BLU
-12	J14-12	AC PHASE C	BLU
P31-A1	J14-A1	+28V DC	WHT

Table G-3. Motherboard Wire List (Semiconductor Processor)

FROM	TO	FUNCTION	COLOR
P31-A1	J14-A1	+ 28V DC	WHT
-A1	J14-A1	+ 28V DC	WHT
-A1	J14-A1	+ 28V DC	WHT
-A1	J14-A1	+ 28V DC	WHT
-A2	J14-A2	– 28V DC	BLK
-A2	J14-A2	– 28V DC	BLK
-A2	J14-A2	– 28V DC	BLK
-A2	J14-A2	– 28V DC	BLK
P31-A2	J14-A2	– 28V DC	BLK
SHIELD	E65	CHASSIS GND	BLK
J14-A1	J17-2	+ 28V DC	WHT
-A2	J17-1	– 28V DC	BLK
-3	J17-4	AC PHASE A	RED
-4	J17-5	AC PHASE B	YEL
J14-1	E70	110 VAC SELECT	BRN
J14-8	E71	110 VAC SELECT	GRA
-2	E72	110 VAC SELECT	RED
J14-9	E73	110 VAC SELECT	WHT
E70	E71	110 VAC STRAP	BLK
E72	E73	110 VAC STRAP	BLK
J14-7	S1-1	RESET RET.	VIO
-14	S1-3	RESET	WHT/YEL
-6	E65	CHASSIS GND	BLK
-13	E65	CHASSIS GND	BLK
J14-5	J17-6	AC PHASE C	BLU
A20J1-A1	A20J1-C2	BNK2ENB*	WHT
A17J1-A1	A17J1-C6	BNK1ENB*	WHT
E35	A8J2-48	INTP	WHT
A2J2-42	A1J2-48	INTP	WHT
A3J2-42	A2J2-48	INTP	WHT
A4J2-42	A3J2-48	INTP	WHT
A5J2-42	A4J2-48	INTP	WHT
A6J2-42	A5J2-48	INTP	WHT
A7J2-42	A6J2-48	INTP	WHT
A8J2-42	A7J2-48	INTP	WHT
A2J2-5	A1J2-4	DCHP	WHT
A3J2-5	A2J2-4	DCHP	WHT
A4J2-5	A3J2-4	DCHP	WHT
A5J2-5	A4J2-4	DCHP	WHT
A6J2-5	A5J2-4	DCHP	WHT
A7J2-5	A6J2-4	DCHP	WHT

Table G-3. Motherboard Wire List (Semiconductor Processor)

FROM	TO	FUNCTION	COLOR
A8J2-5	A7J2-4	DCHP	WHT
E29	A3J2-27	+12V	WHT
E29A	A4J2-27	+12V	WHT
E31	A5J2-27	+12V	WHT
E31A	A6J2-27	+12V	WHT
E33A	A7J2-27	+12V	WHT
E33	A8J2-27	+12V	WHT
E28A	A3J2-25	–12V	WHT
E30	A4J2-25	–12V	WHT
E30A	A5J2-25	–12V	WHT
E32	A6J2-25	-12V	WHT
E32A	A7J2-25	– 12V	WHT
E34	A8J2-25	–12V	WHT
J2-1	A1J1-33	BDATA2*	WHT/ORN
-2	A1J1-37	BDATA1 *	WHT/VIO
-5	A1J1-23	BDATA7*	ORN
-6	A1J1-29	BDATA6*	WHT
-12	A1J1-21	GND	BLK
-12	A1J1-21	GND	BLK
-4	A1J1-34	BDATA8*	WHT/YEL
-Io	A1J1-32	BDATA13*	WHT/RED
-11	A2J1-26	BDATA12*	BLU
-20	A1J1-24	BDATA15*	YEL
-3	A1J1-35	BDATA0*	WHT/GRN
-9	A1J1-27	BDATA3*	VIO
-15	A1J1-36	BDATA10*	WHT/BLU
-16	A1J1-30	BDATA9 *	BLK
J2-14	A1J1-21	GND	BLK
J2-14	A1J1-21	GND	BLK
-7	A1J1-25	BDATA5 *	GRN
-8	A1J1-31	B DATA4 •	WHT/BRN
-13	A1J1-38	BDATA11*	WHT/GRA
-21	A1J1-28	BDATA14*	GRA
-25	A1J1-10	BSELD*	BLK
-26	A1J1-52	BDATOA	WHT/RED
-32	A1J1-20	BDATOC	BLK
-34	A1J1-53	BDATOB	WHT/ORN
-33	A1J1-19	GND	BLK
-40	A1J1-42	BDCHO	RED
-33	A1J1-19	GND	BLK
J2-52	A1J1-7	BDCHI	VIO

Table G-3. Motherboard Wire List (Semiconductor Processor)

FROM	TO	FUNCTION	COLOR
J2-38	A1J1-15	GND	BLK
-17	CHASSIS	CHASSIS GND	BLK
-33	A1J1-19	GND	BLK
-18	A1J1-43	BDS3*	ORN
-19	A1J1-41	BDS4*	BRN
-27	A1J1-45	BD21*	GRN
-28	A1J1-6	BDCHPOUT*	BLU
-41	A1J1-8	BINTR*	GRA
-47	A1J1-44	BRQENB*	YEL
-48	A1J1-16	BDCHMI*	WHT/BLU
-35	A1J1-4	BINTPIN*	YEL
J2-30	A1J1-1	BDATIA	BRN
J2-31	A1J1-3	BDATIC	ORN
-36	A1J1-11	BDCHPIN*	WHT/BRN
-37	A1J1-5	BDATIB	GRN
-39	A1J1-12	BSELB*	WHT/RED
-38	A1J1-17	GND	BLK
-38	A1J1-17	GND	BLK
-22	A1J1-51	BDS5*	WHT/BRN
-23	A1J1-47	BDS2*	VIO
-24	A1J1-13	BINTPOUT*	WHT/ORN
-29	AJ1-49	BDSO*	WHT
-45	A1J1-18	BDCHR*	WHT/GRA
-46	A1J1-9	BDCHA*	WHT
-51	A1J1-14	BDCHMO*	WHT/YEL
-42	A1J1-40	BIOPLS	BLK
-49	A1J1-39	BSTRT	WHT
-50	A1J1-48	BCLR	GRA
-54	A1J1-22	BOVFLO	RED
-43	A1J1-15	GND	BLK
-43	A1J1-15	GND	BLK
-44	A1J1-50	BIORST	BLK
-53	A1J1-46	BMSKO*	BLU
J2-55	A1J1-54	BINTA	WHT/YEL
J3-1	A2J2-33	BDATA2*	WHT/ORN
-2	A2J1-37	BDATA1 •	WHT/VIO
J3-5	A2J1-23	BDATA7*	ORN
J3-6	A2J1-29	BDATA6 *	WHT
-12	A2J1-21	GND	BLK
-12	A2J-21	GND	BLK
J3-4	A2J1-34	BDATA8*	WHT/YEL

Table G-3. Motherboard Wire List (Semiconductor Processor)

FROM	TO	FUNCTION	COLOR
J3-10	A2J1-32	BDATA13*	WHT/RED
-11	A2J1-26	BDATA12*	BLU
-20	A2J1-24	BDATA15*	YEL
-3	A2J1-35	BDATA0*	WHT/GRN
-9	A2J1-27	BDATA3*	VIO
-15	A2J1-36	BDATA10*	WHT/BLU
-16	A2J1-30	BDATA9*	BLK
-14	A2J1-21	GND	BLK
-14	A2J1-21	GND	BLK
-7	A2J1-25	BDATA5*	GRN
-8	A2J1-31	BDATA4*	WHT/BRN
-13	A2J1-38	BDATA11*	WHT/GRA
-21	A2J1-28	BDATA14*	GRA
-25	A2J1-10	BSELD*	BLK
-26	A2J1-52	BDATOA	WHT/RED
-32	A2J1-20	BDATOC	BLK
-34	A2J1-53	BDATOB	WHT/ORN
-33	A2J1-19	GND	BLK
-40	A2J1-42	BDCHO	RED
J3-33	A2J1-19	GND	BLK
J3-52	A2J1-7	BDCHI	VIO
-38	A2J1-15	GND	BLK
-17	CHASSIS	CHASSIS GND	BLK
-33	A2J1-19	GND	BLK
-18	A2J1-43	BDS3*	ORN
-19	A2J1-41	BDS4*	BRN
-27	A2J1-45	BD21*	GRN
-28	A2J1-6	BDCHPOUT*	BLU
-41	A2J1-8	BINTR*	GRA
-47	A2J1-44	BRQENB*	YEL
-48	A2J1-16	BDCHMI*	WHT/BLU
-35	A2J1-4	BINTPIN*	YEL
-30	A2J11	BDATIA	BRN
-31	A2J1-3	BDATIC	ORN
-36	A2J111	BDCHPIN*	WHT/BRN
-37	A2J1-5	BDATIB	GRN
-39	A2J1-12	BSELB*	WHT/RED
-38	A2J1-17	GND	BLK
-38	A2J1-17	GND	BLK
-22	A2J1-51	BDS5*	WHT/BRN
J3-23	A2J1-47	BDS2*	VIO

Table G-3. Motherboard Wire List (Semiconductor Processor)

FROM	TO	FUNCTION	COLOR
J3-24	A2J1-13	BINTPOUT*	WHT/ORN
-29	A2J1-49	BDSO*	WHT
-45	A2J1-18	BDCHR*	WHT/GRA
-46	A2J1-9	BDCHA*	WHT
-51	A2J1-14	BDCHMO”	WHT/YEL
-42	A2J1-40	BIOPLS	BLK
-49	A2J1-39	BSTRT	WHT
J3-50	A2J1-48	BCLR	GRA
J3-54	A2J1-22	BOVFLO	RED
-43	A2J1-15	GND	ELK
-43	A2J1-15	GND	ELK
-44	A2J1-50	BIORST	ELK
-53	A2J1-46	BMSKO*	BLU
J3-55	A2J1-54	BINTA	WHT/YEL
J4-1	A3J1-1	GND	BRN
-2	A3J1-2		RED
-3	A3J1-3		ORN
-4	A3J1-4		YEL
-5	A3J1-5		GRN
-6	A3J1-6		BLU
-7	A3J1-7		VIO
-8	A3J1-8		GRA
-9	A3J1-9		WHT
-10	A3J1-10		BLK
-11	A3J1-11		WHT/BRN
-12	A3J1-12		WHT/RED
-13	A3J1-13	GN13	WHT/ORN
-14	A3J1-14		WHT/YEL
-15	A3J1-15		WHT/GRN
-16	A3J1-16		WHT/BLU
-17	A3J1-17		WHT/VIO
-18	A3J1-18		WHT/GRA
-19	A3J1-19		WHT
-20	A3J1-20		BLK
-21	A3J1-21		BRN
-22	A3J1-22		RED
J4-23	A3J1-23		ORN
J4-24	A3J1-24		YEL
-25	A3J1-25		GRN
-26	A3J1-26		BLU
J4-27	A3J1-27		VIO

Table G-3. Motherboard Wire List (Semiconductor Processor)

FROM	TO	FUNCTION	COLOR
J4-28	A3J1-28		GRA
-29	A3J1-29		WHT
-30	A3J1-30		BLK
-31	A3J1-31		WHT/BRN
-32	A3J1-32		WHT/RED
-33	A3J1-33		WHT/ORN
-34	A3J1-34	GND	WHT/YEL
-35	A3J1-35		WHT/GRN
-36	A3J1-36		WHT/BLU
-37	A3J1-37		WHT/VIO
-38	A3J1-38		WHT/GRA
-39	A3J1-39		WHT
-40	A3J1-40		BLK
-41	A3J1-41		BRN
-42	A3J1-42		RED
-43	A3J1-43		ORN
-44	A3J1-44		YEL
-45	A3J1-45		GRN
-46	A3J1-46		BLU
-47	A3J1-47		VIO
-48	A3JI-48		GRA
-49	A3J1-49		WHT
-50	A3J1-50		BLK
-51	A3J1-51		WHT/BRN
J4-52	A3J1-52		WHT/RED
J4-53	A3J1-53	GND	WHT/ORN
-54	A3J1-54		WHT/YEL
J4-55	CHASSIS	CHASSIS GND	BLK
J5-1	A4J1-1	GND	BRN
-2	A4J1-2		RED
-3	A4J1-3		ORN
-4	A4J1-4		YEL
-5	A4J1-5		GRN
-6	A4J1-6		BLU
-7	A4J1-7		VIO
-8	A4J1-8		GRA
-9	A4J1-9		WHT
10	A4J1-10		BLK
-11	A4J1-11		WHT/BRN
-12	A4J1-12		WHT/RED
J5-13	A4J1-13	GND	WHT/ORN

Table G-3. Motherboard Wire List (Semiconductor Processor)

FROM	TO	FUNCTION	COLOR
J5-14	A4J1-14		WHT/YEL
-15	A4J1-15		WHT/GRN
-16	A4J1-16		WHT/BLU
-17	A4J1-17		WHT/VIO
-18	A4J1-18		WHT/GRA
-19	A4J1-19		WHT
-20	A4J1-20		BLK
-21	A4J1-21		BRN
-22	A4J1-22		RED
-23	A4J1-23		ORN
-24	A4J1-24		YEL
-25	A4J1-25		GRN
J5-26	A4J1-26		BLU
J5-27	A4J1-27		VIO
-28	A4J1-28		GRA
-29	A4J1-29		WHT
-30	A4J1-30		BLK
-31	A4J1-31		WHT/BRN
-32	A4J1-32		WHT/RED
-33	A4J1-33		WHT/ORN
-34	A4J1-34	GND	WHT/YEL
-35	A4J1-35		WHT/GRN
-36	A4J1-36		WHT/BLU
-37	A4J1-37		WHT/VIO
-38	A4J1-38		WHT/GRA
-39	A4J1-39		WHT
-40	A4J1-40		BLK
-41	A4J1-41		BRN
-42	A4J1-42		RED
-43	A4J1-43		ORN
-44	A4J1-44		YEL
-45	A4J1-45		GRN
-46	A4J1-46		BLU
-47	A4J1-47		VIO
-48	A4J1-48		GRA
-49	A4J1-49		WHT
-50	A4J1-50		BLK
-51	A4J1-51		WHT/BRN
-52	A4J1-52		WHT/RED
-53	A4J1-53	GND	WHT/ORN
J5-54	A4J1-54		WHT/YEL

Table G-3. Motherboard Wire List (Semiconductor Processor)

FROM	TO	FUNCTION	COLOR
J5-55	CHASSIS	CHASSIS GND	BLK
J7--1	A5J1-1	GND	BRN
-2	A5J1-2		RED
-3	A5J1-3		ORN
-4	A5J1-4		YEL
-5	A5J1-5		GRN
-6	A5J1-6		BLU
-7	A5J1-7		VIO
-8	A5J1-8		GRA
-9	A5J1-9		WHT
-10	A5J1-10		BLK
-11	A5J1-11		WHT/BRN
-12	A5J1-12		WHT/RED
-13	A5J1-13	GND	WHT/ORN
-14	A5J1-14		WHT/YEL
-15	A5J1-15		WHT/GRN
-16	A5J1-16		WHT/BLU
-17	A5J1-17		WHT/VIO
-18	A5J1-18		WHT/GRN
-19	A5J1-19		WHT
-20	A5J1-20		BLK
-21	A5J1-21		BRN
-22	A5J1-22		RED
-23	A5J1-23		ORN
-24	A5J1-24		YEL
-25	A5J1-25		GRN
-26	A5J1-26		BLU
-27	A5J1-27		VIO
-28	A5J1-28		GRA
J7-29	A5J1-29		WHT
J7-30	A5J1-30		BLK
-31	A5J1-31		WHT/BRN
-32	A5J1-32		WHT/RED
-33	A5J1-33		WHT/ORN
-34	A5J1-34	GND	WHT/YEL
-35	A5J1-35		WHT/GRN
-36	A5J1-36		WHT/BLU
-37	A5J1-37		WHT/VIO
-38	A5J1-38		WHT/GRA
-39	A5J1-39		WHT
-40	A5J1-40		BLK

Table G-3. Motherboard Wire List (Semiconductor Processor)

FROM	TO	FUNCTION	COLOR
J7-41	A5J1-41		BRN
-42	A5J1-42		RED
-43	A5J1-43		ORN
-44	A5J1-44		YEL
-45	A5J1-45		GRN
-46	A5J1-46		BLU
-47	A5J1-47		VIO
-48	A5J1-48		GRN
-49	A5J1-49		WHT
-50	A5J1-50		BLK
-51	A5J1-51		WHT/BRN
-52	A5J1-52		WHT/RED
-53	A5J1-53	GND	WHT/ORN
-54	A5J1-54		WHT/YEL.
J 7-55	CHASSIS	CHASSIS GND	BLK
J8-1	A6J1-1	GND	BRN
-2	A6J1-2		RED
J8-3	A6J1-3		ORN
J8-4	A6J1-4		YEL
-5	A6J1-5		GRN
-6	A6J1-6		BLU
-7	A6J1-7		VIO
-8	A6J1-8		GRA
-9	A6J1-9		WHT
-10	A6JI-10		BLK
-11	A6J1-11		WHT/BRN
-12	A6J1-12		WHT/RED
-13	A6J1-13	GND	WHT/ORN
-14	A6J1-14		WHT/YEL
-15	A6J1-15		WHT/GRN
-16	A6JI-16		WHT/BLU
-17	A6J1-17		WHT/VIO
-18	A6J1-18		WHT/GRA
-19	A6J1-19		WHT
-20	A6J1-20		BLK
-21	A6J1-21		BRN
-22	A6J1-22		RED
-23	A6J1-23		ORN
-24	A6J1-24		YEL
-25	A6J1-25		GRN
J8-26	A6J1-26		BLU

Table G-3. Motherboard Wire List (Semiconductor Processor)

FROM	TO	FUNCTION	COLOR
J8-27	A6J1-27		VIO
-28	A6J1-28		GRA
-29	A6J1-29		WHT
-30	A61J-30		BLK
-31	A6J1-31		WHT/BRN
J8-32	A6J1-32		WHT/RED
J8-33	A6J1-33		WHT.ORN
-34	A6J1-34		WHT/YEL
-35	A6J1-35	GND	WHT/GRN
-36	A6J1-36		WHT/BLU
-37	A6J1-37		WHT/VIO
-38	A6J1-38		WHT/GRA
-39	A6J1-39		WHT
-40	A6J1-40		BLK
-41	A6J1-41		BRN
-42	A6J1-42		RED
-43	A6J1-43		ORN
-44	A6J1-44		YEL
-45	A6J1-45		GRN
-46	A6J1-46		BLU
-47	A6J1-47		VIO
-48	A6J1-48		GRA
-49	A6J1-49		WHT
-50	A6J1-50		BLK
-51	A6J1-51		WHT/BRN
-52	A6J1-52		WHT/RED
-53	A6J1-53	GND	WHT/ORN
-54	A6J1-54		WHT/YEL
J8-55	CHASSIS	CHASSIS GND	BLK
J9-1	A7J1-1	GND	BRN
-2	A7J1-2		RED
-3	A7J1-3		ORN
-4	A7J1-4		YEL
-5	A7J1-5		GRN
J9-6	A7J1-6		BLU
J9-7	A7J1-7		VIO
-8	A7J1-8		GRA
-9	A7J1-9		WHT
-10	A7J1-10		BLK
-11	A7J1-11		WHT/BRN
J9-12	A7J1-12		WHT/RED

Table G-3. Motherboard Wire List (Semiconductor Processor)

FROM	TO	FUNCTION	COLOR
J9-13	A7J1-13	GND	WHT/ORN
-14	A7J1-14		WHT/YEL
-15	A7J1-15		WHT/GRN
-16	A7J1-16		WHT/BLU
-17	A7J1-17		WHT/VIO
-18	A7J1-18		WHT/GRA
-19	A7J1-19		WHT
-20	A7J1-20		BLK
-21	A7J1-21		BRN
-22	A7J1-22		RED
-23	A7J1-23		ORN
-24	A7J1-24		YEL
-25	A7J1-25		GRN
-26	A7J1-26		BLU
-27	A7J1-27		VIO
-28	A7J1-28		GRA
-29	A7J1-29		WHT
-30	A7J1-30		BLK
-31	A7J1-31		WHT/BRN
-32	A7J1-32		WHT/RED
-33	A7J1-33		WHT/ORN
-34	A7J1-34	GND	WHT/YEL
J9-35	A7J1-35		WHT/GRN
J9-36	A7J1-36		WHT/BLU
-37	A7J1-37		WHT/VIO
-38	A7J1-38		WHT/GRA
-39	A7J1-39		WHT
-40	A7J1-40		BLK
-41	A7J1-41		BRN
-42	A7J1-42		RED
-43	A7J1-43		ORN
-44	A7J1-44		YEL
-45	A7J1-45		GRN
-46	A7J1-46		BLU
-47	A7J1-47		VIO
-48	A7J1-48		GRA
-49	A7J1-49		WHT
-50	A7J1-50		BLK
-51	A7J1-51		WHT/BRN
-52	A7J1-52		WHT/RED
J9-53	A7J1-53	GND	WHT/ORN

Table G-3. Motherboard Wire List (Semiconductor Processor)

FROM	TO	FUNCTION	COLOR
J9-54	A7J1-54		WHT/YEL
-55	CHASSIS	CHASSIS GND	BLK
J10-1	A8J1-1		BRN
-2	A8J1-2		RED
-3	A8J1-3		ORN
-4	A8J1-4		YEL
-5	A8J1-5		GRN
-6	A8J1-6		BLU
-7	A8J1-7		VIO
-8	A8J1-8		GRA
J10-9	A8J1-9		WHT
J10-10	A8J1-10		BLK
-11	A8J1-11		WHT/BRN
-12	A8J1-12		WHT/RED
-13	A8J1-13	GND	WHT/ORN
-14	A8J1-14		WHT/YEL
15	A8JI-15		WHT/GRN
-16	A8J1-16		WHT/BLU
-17	A8J1-17		WHT/VIO
-18	A8J1-18		WHT/GRA
-19	A8J1-19		WHT
-20	A8J1-20		BLK
21	A8J1-21		BRN
-22	A8J1-22		RED
-23	A8J1-23		ORN
-24	A8J1-24		YEL
-25	A8J1-25		GRN
-26	A8J1-26		BLU
-27	A8J1-27		VIO
-28	A8J1-28		GRA
-29	A8J1-29		WHT
-30	A8J1-30		BLK
-31	A8J1-31		WHT/BRN
-32	A8J1-32		WHT/RED
-33	A8J1-33		WHT/ORN
-34	A8J1-34	GND	WHT/YEL
-35	A8J1-35		WHT/GRN
-36	A8J1-36		WHT/BLU
-37	A8J1-37		WHT/VIO
-38	A8J1-38		WHT/GRA
J10-39	A8J1-39		WHT

Table G-3. Motherboard Wire List (Semiconductor Processor)

FROM	TO	FUNCTION	COLOR
J10-40	A8J1-40		BLK
-41	A8J1-41		BRN
-42	A8J1-42		RED
-43	A8J1-43		ORN
-44	A8J1-44		YEL
-45	A8J1-45		GRN
-46	A8J1-46		BLU
-47	A8J1-47		VIO
-48	A8J1-48		GRA
-49	A8J1-49		WHT
-50	A8J1-50		BLK
-51	A8J1-51		WHT/BRN
-52	A8J1-52		WHT/RED
-53	A8J1-53	GND	WHT/ORN
-54	A8J1-54		WHT/YEL
J10-55	CHASSIS	CHASSIS GND	BLK

Table G-4. Motherboard Wire List (Core Memory Processor)

FROM	TO	FUNCTION	COLOR
J11-1	GND BY A8J2-4	GND	BLK
-2	E32-1	-12V	BRN
-3	NC		
-4	E33-2	CTSIN	RED
-5	NC		
-6	E33-4	TTIN	YEL
-7	NC		
-8	NC		
-9	NC		
-10	E33-8	RDRRUN	GRA
-11	E33-3	EXTCLK	ORN
-12	NC		
-13	E60	GND	BLK
-14	E60	GND	BLK
-15	NC		
-16	NC		
-17	E33-1	CTSOUT	BRN
-18	NC		
-19	E33-5	TTOUT	GRN
-20	E32-2	+V12	RED
-21	NC		
-22	NC		
-23	NC		
-24	NC		
-25	S2-3	PRST*	ORN
-26	S2-1	GND	BLK
-27	NC		
-28	M1(+)		RED
-29	NC		
-30	S3-3	CONPL*	ORN
-31	S3-1	GND	BLK
-32	E33-6	CONLOCK*	BLU
-33	E60	GND	BLK
-34	NC		
-35	NC		
-36	NC		
-37	NC		
-38	NC		
-39	S2-4	RUN LITE	YEL
-40	S3-4	BITE*	WHT/YEL
J11-41	NC		

Table G-4. Motherboard Wire List (Core Memory Processor)-Continued

FROM	TO	FUNCTION	COLOR
J11-42	NC		
-43	NC		
-44	NC		
-45	NC		
-46	NC		
-47	NC		
-48	NC		
-49	NC		
-50	NC		
-51	NC		
-52	NC		
-53	NC		
-54	NC		
J11-55	CHASSIS	CHASSIS GND	BLK
J6-1	A9J1-A30	GND	BLK
-6	A10J1-A30	GND	BLK
-2	E21-16	ED0P*	WHT/BLU
-7	E21-15	ED0N	WHT/GRN
-3	E21-18	ED1N*	WHT/GRA
-8	A21-17	ED1P*	WHT/VIO
-4	E21-20	ED2P*	BLK
-5	E21-19	ED2N *	WHT
-9	E21-22	ED3P*	RED
-16	E21-21	ED3N *	BRN
-10	E21-24	ED4P*	YEL
-11	E21-23	ED4N *	ORN
-12	E21-26	ED5P*	BLU
-13	E21-25	ED5N*	GRN
-14	E21-28	ED6P*	GRA
-15	E21-27	ED6N*	VIO
-17	E21-30	ED7P*	BLK
-18	E21-29	ED7N*	WHT
-19	E21-32	ED8P*	WHT/RED
-20	E21-31	ED8N*	WHT/BRN
-21	E21-34	ED9P*	WHT/YEL
-22	E21-33	ED9N*	WHT/ORN
-23	E21-36	EDI0P*	WHT/BLU
-24	E21-35	ED10N*	WHT/GRN
-25	E21-38	ED11P*	WHT/GRA
-32	E21-37	ED11N*	WHT/VIO
J6-26	E21-40	ED12P*	BLK

Table G-4. Motherboard Wire List (Core Memory Processor)-Continued

FROM	TO	FUNCTION	COLOR
J6-27	E21-39	ED12N*	WHT
-28	E21-42	ED13P*	RED
-29	E21-41	ED13N*	BRN
-30	E21-44	ED14P*	YEL
-31	E21-43	ED14N*	ORN
-33	E21-46	ED15P*	BLU
-34	E21-45	ED15N*	GRN
-35	E34-8	WRQP*	GRA
-36	E34-7	WRQN*	VlO
-37	E34-10	RRQP*	BLK
-38	E34-9	RRQN*	WHT
-39	CHASSIS	CHASSIS GND	BLK
-40	E34-4	AAKP*	YEL
-41	E34-3	AAKN*	ORN
-42	E34-6	DAKP*	BLU
-43	E34-5	DAKN*	GRN
-44	E21-12	INRP*	WHT/RED
-45	E21-11	IN RN*	WHT/BRN
-46	E21-2	MAOP*	RED
-52	E21-1	MAON*	BRN
-47	E21-4	MA1P*	YEL
-48	E21-3	MA1N*	ORN
-49	E21-6	MA2P*	BLU
-53	E21-5	MA2N*	GRN
-50	E21-8	MA3P*	GRA
-54	E21-7	MA3N*	VlO
-51	E21-47	RDCHSN*	VlO
J6-55	E21-48	RDCHSP*	GRA
J15-1	NC		
-2	NC		
-3	E38	-5V	ORN
-4	E39	-5V	YEL
-5	E29	-12V	GRN
-6	E29A	-12V	BLU
-7	NC		
-8	NC		
-9	E35	+ 12V	WHITE
-10	E35A	+12V	WHT/BLK
-11	E9	+5V SNS RET	WHT/BRN
-12	E10	+5V SNS	WHT/RED
.J15-13	NC		

Table G-4. Motherboard Wire List (Core Memory Processor). Continued

FROM	TO	FUNCTION	COLOR
J15-14	NC		
-15	E21-10	+5V OK	WHT/GRN
-16	E21-9	MEM OK	WHT/BLU
-17	E20-7	PWR FAIL	WHT/VIO
-A1	E18	AUX V. RET	BLK
-A1	E16	AUX V. RET	BLK
-A2	E2	+5V RET	BLK
-A2	E2	+5V RET	BLK
-A2	E6	+5V RET	BLK
-A3	E8	+5V RET	BLK
-A3	E12	+5V RET	BLK
-A3	E14	+5V RET	BLK
-A4	E1	+ 5V	WHT
-A4	E3	+ 5V	WHT
-A4	E5	+ 5V	WHT
-A4	E7	+ 5V	WHT
-A5	E11	+ 5V	WHT
-A5	E13	+ 5V	WHT
-A5	E15	+ 5V	WHT
-A5	E17	+ 5V	WHT
-A6	E19	+15V	GRA
J15-A6	E19A	+15V	GRA
E60	E20-4	GND	BLK
E60	E36-1	GND	BLK
S1-4	E60	GND	BLK
S1-2	E36-2	+ 5V	RED
S2-3	E20-3	PRST	ORN
-1	E60	GND	BLK
-2	E20-5	+ 5V	RED
S2-4	A12J1-C9	CONSOLMODE	WHT
S3-2	E20-2	+ 5V	RED
-4	E20-1	BITE	WHT/RED
-1	E60	GND	BLK
S3-3	E33-7	CONPL	ORN
M1(+)	E1A	+ 5V	RED
M1(-)	E2A	GND	BLK
P13-3	J 14-3	AC PHASE A	RED
-10	J14-10	AC PHASE A	RED
-4	J14-4	AC PHASE B	YEL
-11	J14-11	AC PHASE B	YEL
P13-5	J14-5	AC PHASE C	BLU

Table G-4. Motherboard Wire List (Core Memory Processor)-Continued

FROM	TO	FUNCTION	COLOR
P13-12	J14-12	AC PHASE C	BLU
-A1	J14-A1	+28V DC	WHT
-A1	J14-A1	+28V DC	WHT
-A1	J14-A1	+ 28V DC	WHT
-A1	J14-A1	+ 28V DC	WHT
-A1	J14-A1	+28V DC	WHT
-A2	J14-A2	-28V DC	BLK
-A2	J14-A2	-28V DC	BLK
-A2	J14-A2	-28V DC	BLK
-A2	J14-A2	-28V DC	BLK
P13-A2	J14-A2	-28V DC	BLK
J14-A1	J17-2	+28V DC	WHT
SHIELD	E65	CHASSISGND	BLK
-A2	J17-1	28V DC	BLK
-3	J17-4	AC PHASE A	RED
-4	J17-5	AC PHASE B	YEL
-1	E70	110VAC SELECT	BRN
-8	E71	110VAC SELECT	GRA
-2	E72	110VAC SELECT	RED
J 14-9	E73	110VAC SELECT	WHT
E70	E71	110VAC STRAP	BLK
E72	E73	110VAC STRAP	BLK
J14-7	S1-1	RESET RET.	VIO
-14	S1-3	RESET	WHT/YEL
-6	E65	CHASSISGND	BLK
J14-13	E65	CHASSISGND	BLK
E37	A8J2-48	INTP*	WHT
A2J2-42	A1J2-48	INTP*	WHT
A3J2-42	A2J2-48	INTP'	WHT
A4J2-42	A3J2-48	INTP*	WHT
A5J2-42	A4J2-48	INTP*	WHT
A6J2-42	A5J2-48	INTP*	WHT
A7J2-42	A6J2-48	INTP*	WHT
A8J2-42	A7J2-48	INTP'	WHT
A2J2-5	A1J2-4	DCHP*	WHT
A3J2-5	A2J2-4	DCHP*	WHT
A4J2-5	A3J2-4	DCHP*	WHT
A5J2-5	A4J2-4	DCHP*	WHT
A6J2-5	A5J2-4	DCHP*	WHT
A7J2-5	A6J2-4	DCHP*	WHT
A8J2-5	A7J2-4	DCHP*	WHT

Table G-4. Motherboard Wire List (Core Memory Processor)-Continued

FROM	TO	FUNCTION	COLOR
J2-1	A1J1-33	BDATA2*	WHT/ORN
-2	A1J1-37	BDATA1 *	WHT/VIO
-5	A1J1-23	BDATA7 *	ORN
-6	A1J1-29	BDATA6*	WHT
-12	A1J1-21	GND	BLK
-12	A1J1-21	GND	BLK
-4	A1J1-34	BDATA8	WHT/YEL
-10	A1J1-32	BDATA13*	WHT/RED
-11	A1J1-26	BDATA12*	BLU
-20	A1J1-24	BDATA15*	YEL
-3	A1J1-35	BDATA0*	WHT/GRN
-9	A1J1-27	BDATA3*	VIO
-15	A1J1-36	BDATA10*	WHT/BLU
-16	A1J1-30	BDATA9*	BLK
-14	A1J1-21	GND	BLK
-14	A1J1-21	GND	BLK
-7	A1J1-25	BDATA5*	GRN
-8	A1J1-31	BDATA4*	WHT/BRN
-13	A1J1-38	BDATA11*	WHT/GRA
-21	A1J1-28	BDATA14*	GRA
-25	A1J1-10	BSELD*	BLK
-26	A1J1-52	BDATOA	WHT/RED
-32	A1J1-20	BDATOC	BLK
-34	A1J1-53	BDATOB	WHT/ORN
-33	A1J1-19	GND	BLK
-40	A1J1-42	BDCHO	RED
-33	A1J1-19	GND	BLK
-52	A1J1-7	BDCHI	VIO
-38	A1J1-15	GND	BLK
-17	CHASSIS	CHASSIS GND	BLK
-33	A1J1-19	GND	BLK
-18	A1J1-43	BDS3*	ORN
-19	A1J1-41	BDS4*	BRN
-27	A1J1-45	BD21*	GRN
-28	A1J1-6	BDCHPOUT*	BLU
-41	A1J1-8	BINTR*	GRA
-47	A1J1-44	BRQENB*	YEL
-48	A1J1-16	BDCHMI*	WHT/BLU
-35	A1J1-4	BINTPIN*	YEL
-30	A1J1-1	BDATIA*	BRN
J2-31	A1J1-3	BDATIC	ORN

Table G-4. Motherboard Wire List (Core Memory Processor)-Continued

FROM	TO	FUNCTION	COLOR
J2-36	A1J1-11	BDCHPIN	WHT/BRN
-37	A1J1-5	BDATIB	GRN
-39	A1J1-12	BSELB*	WHT/RED
-38	A1J1-17	GND	BLK
-38	A1J1-17	GND	BLK
-22	A1J1-51	BDS5*	WHT/BRN
-23	A1J1-47	BDS2*	VIO
-24	A1J1-13	BINTPOUT*	WHT/ORN
-29	A1J1-49	BDSO*	WHT
-45	A1J1-18	BDCHR*	WHT/GRA
-46	A1J1-9	BDCHA*	WHT
-51	A1J1-14	BDCHM0*	WHT/YEL
-42	A1J1-40	BIOPLS	BLK
-49	A1J1-39	BSTRT	WHT
-50	A1J1-48	BCLR	GRA
-54	A1J1-22	BOVFLO	RED
-43	A1J1-15	GND	BLK
J2-43	A1J1-15	GND	BLK
J2-44	A1J1-50	BIORST	BLK
-53	A1J1-46	BMSKO*	BLU
J2-55	A1J1-54	BINTA	WHT/YEL
J3-1	A2J1-33	BDATA2*	WHT/ORN
-2	A2J1-37	BDATA1*	WHT/VIO
-5	A2J1-23	BDATA7*	ORN
-6	A2J1-29	BDATA6 *	WHT
-12	A2J1-21	GND	BLK
-12	A2J1-21	GND	BLK
-4	A2J1-34	B DATA8*	WHT/YEL
-10	A2J1-32	BDATA13*	WHT/RED
-11	A2J1-26	BDATA12*	BLU
-20	A2J1-24	BDATA15*	YEL
-3	A2J1-35	BDATA0*	WHT/GRN
-9	A2J1-27	BDATA3*	VIO
-15	A2J1-36	BDATA10*	WHT/BLU
-16	A2J1-30	BDATA9*	BLK
-14	A2J1-21	GND	BLK
-14	A2J1-21	GND	BLK
-7	A2J1-25	BDATA5*	GRN
-8	A2J1-31	BDATA4 *	WHT/BRN
-13	A2J1-38	BDATA11*	WHT/GRA
J3-21	A2J1-28	BDATA14*	GRA

Table G-4. Motherboard Wire List (Core Memory Processor)-Contlnued

FROM	TO	FUNCTION	COLOR
J3-25	A2J1-10	BSELD*	BLK
-26	A2J1-52	BDATOA	WHT/RED
-32	A2J1-20	BDATOC	BLK
-34	A2J1-53	BDATOB	WHT/ORN
-33	A2J1-19	GND	BLK
J3-40	A2J1-42	BDCHO	RED
J3-33	A2J1-19	GND	BLK
-52	A2J1-7	BDCHI	VIO
-38	A2J1-15	GND	BLK
-17	CHASSIS	CHASSIS GND	BLK
-33	A2J1-19	GND	BLK
-18	A2J1-43	BDS3	ORN
-19	A2J1-41	BDS4	BRN
-27	A2J1-45	BDSI	GRN
-28	A2J1-6	BDCHPOUT	BLU
-41	A2J1-8	BINTR	GRA
-47	A2J1-44	BRQENB	YEL
-48	A2J1-16	BDCHMI	WHT/BLU
-35	A2J1-4	BINTPIN	YEL
-30	A2J1-1	BDATIA	BRN
-31	A2J1-3	BDATIC	ORN
-36	A2J1-11	BDCHPIN	WHT/BRN
-37	A2J1-5	BDATIB	GRN
-39	A2J1-12	BSELB	WHT/RED
-38	A2J1-17	GND	BLK
-38	A2J1-17	GND	BLK
-22	A2J1-51	BDS5	WHT/BRN
-23	A2J1-47	BDS2	VIO
-24	A2J1-13	BINTPOUT	WHT/ORN
-29	A2J1-49	BDSO	WHT
-45	A2J1-18	BDCHR	WHT/GRA
-46	A2J1-9	BDCHA	WHT
-51	A2J1-14	BDCHMO	WHT/YEL
-42	A2J1-40	BIOPLS	BLK
J3-49	A2J1-39	BSTRT	WHT
J3-50	A2J1-48	BCLR	GRA
-54	A2J1-22	BOVFLO	RED
-43	A2J1-15	GND	BLK
-43	A2J1-15	GND	BLK
-44	A2J1-50	BIORST	BLK
J3-53	A2J1-46	BMSKO	BLU

Table G-4. Motherboard Wire List (Core Memory Processor)-Continued

FROM	TO	FUNCTION	COLOR
J3-55	A2J1-54	BINTA	WHT/YEL
J4-1	A3J1-1	GND	BRN
-2	A3J1-2		RED
-3	A3J1-3		ORN
-4	A3J1-4		YEL
-5	A3J1-5		GRN
-6	A3J1-6		BLU
-7	A3J1-7		VIO
-8	A3J1-8		GRA
-9	A3J1-9		WHT
-10	A3J1-10		BLK
-11	A3J1-11		WHT/BRN
-12	A3J1-12		WHT/RED
-13	A3J1-13	GND	WHT/ORN
-14	A3J1-14		WHT/YEL
-15	A3J1-15		WHT/GRN
-16	A3J1-16		WHT/BLU
-17	A3J1-17		WHT/VIO
-18	A3J1-18		WHT/GRA
-19	A3J1-19		WHT
-20	A3J1-20		BLK
-21	A3J1-21		BRN
J4-22	A3J1-22		RED
J4-23	A3J1-23		ORN
-24	A3J1-24		YEL
-25	A3J1-25		GRN
-26	A3J1-26		BLU
-27	A3J1-27		VIO
-28	A3J1-28		GRA
-29	A3J1-29		WHT
-30	A3J1-30		BLK
-31	A3J1-31		WHT/BRN
-32	A3J1-32		WHT/RED
-33	A3J1-33		WHT/ORN
-34	A3J1-34	GND	WHT/YEL
-35	A3J1-35		WHT/GRN
-36	A3J1-36		WHT/BLU
-37	A3J1-37		WHT/VIO
-38	A3J1-38		WHT/GRA
-39	A3J1-39		WHT
J4-40	A3J1-40		BLK

Table G-4. Motherboard Wire List (Core Memory Processor)-Continued

FROM	TO	FUNCTION	COLOR
J4-41	A3J1-41		BRN
-42	A3J1-42		RED
-43	A3J1-43		ORN
-44	A3J1-44		YEL
-45	A3J1-45		GRN
-46	A3J1-46		BLU
-47	A3J1--47		VIO
-48	A3J1-48		GRA
-49	A3J1-49		WHT
-50	A3J1-50		BLK
J4-51	A3J1-51		WHT/BRN
J4-52	A3J1-52		WHT/RED
-53	A3J1-53	GND	WHT/ORN
-54	A3J1-54		WHT/YEL
J4-55	CHASSIS	CHASSIS GND	BLK
J5-1	A4J1-1	GND	BRN
-2	A4J1-2		RED
-3	A4J1-3		ORN
-4	A4J1-4		YEL
-5	A4J1-5		GRN
-6	A4J1-6		BLU
-7	A4J1-7		VIO
-8	A4J1-8		GRA
-9	A4J1-9		WHT
-10	A4J1-10		BLK
-11	A4J1-11		WHT/BRN
-12	A4J1-12		WHT/RED
-13	A4J1-13	GND	WHT/ORN
-14	A4J1-14		WHT/YEL
-15	A4J1-15		WHT/GRN
-16	A4J1-16		WHT/BLU
-17	A4J1-17		WHT/VIO
-18	A4J1-18		WHT/GRA
-19	A4J1-19		WHT
-20	A4J1-20		BLK
-21	A4J1-21		BRN
-22	A4J1-22		RED
-23	A4J1-23		ORN
-24	A4J1-24		YEL
-25	A4J1-25		GRN
J5-26	A4J1-26		BLU

Table G-4. Motherboard Wire List (Core Memory Processor)-Continued

FROM	TO	FUNCTION	COLOR
J5-27	A4J1-27		VIO
-28	A4J1-28		GRA
-29	A4J1-29		WHT
-30	A4J1-30		BLK
-31	A4J1-31		WHT/BRN
-32	A4J1-32		WHT/RED
-33	A4J1-33		WHT/ORN
-34	A4J1-34	GND	WHT/YEL
-35	A4J1-35		WHT/GRN
-36	A4J1-36		WHT/BLU
-37	A4J1-37		WHT/VIO
-38	A4J1-38		WHT/GRA
-39	A4J1-39		WHT
-40	A4J1-40		BLK
-41	A4J1-41		BRN
-42	A4J1-42		RED
-43	A4J1-43		ORN
-44	A4J1-44		YEL
-45	A4J1-45		GRN
-46	A4J1-46		BLU
-47	A4J1-47		VIO
-48	A4J1-48		GRA
-49	A4J1-49		WHT
-50	A4J1-50		BLK
-51	A4J1-51		WHT/BRN
-52	A4J1-52		WHT/RED
-53	A4J1-53	GND	WHT/ORN
-54	A4J1-54		WHT/YEL
J5-55	CHASSIS	CHASSIS GND	BLK
J7-1	A5J1-1	GND	BRN
-2	A5J1-2		RED
-3	A5J1-3		ORN
-4	A5J1-4		YEL
-5	A5J1-5		GRN
-6	A5J1-6		BLU
-7	A5J1-7		VIO
-8	A5J1-8		GRA
-9	A5J1-9		WHT
-10	A5J1-10		BLK
-11	A5J1-11		WHT/BRN
J7-12	A5J1-12		WHT/RED

Table G=4. Motherboard Wire List (Core Memory Processor)-Continued

FROM	TO	FUNCTION	COLOR
J7-13	A5J1-13	GND	WHT/ORN
-14	A5J1-14		WHT/YEL
-15	A5J1-15		WHT/GRN
-16	A5J1-16		WHT/BLU
-17	A5J1-17		WHT/VIO
-18	A5J1-18		W HT/GRA
-19	A5J1-19		WHT
-20	A5J1-20		BLK
-21	A5J1-21		BRN
-22	A5J1-22		RED
-23	A5J1-23		ORN
-24	A5J1-24		YEL
-25	A5J1-25		GRN
-26	A5J1-26		BLU
-27	A5J1-27		VIO
-28	A5J1-28		GRA
J7-29	A5J1-29		WHT
J7-30	A5J1-30		BLK
-31	A5J1-31		WHT/BRN
-32	A5J1-32		WHT/RED
-33	A5J1-33		WHT/ORN
-34	A5J1-34	GND	WHT/YEL
-35	A5J1-35		WHT/GRN
-36	A5J1-36		WHT/BLU
-37	A5J1-37		WHT/VIO
-38	A5J1-38		WHT/GRA
-39	A5J1-39		WHT
-40	A5J1-40		BLK
-41	A5J1-41		BRN
-42	A5J1-42		RED
-43	A5J1-43		ORN
-44	A5J1-44		YEL
-45	A5J1-45		GRN
-46	A5J1-46		BLU
-47	A5J1-47		VIO
-48	A5J1-48		GRA
-49	A5J1-49		WHT
-50	A5J1-50		BLK
-51	A5J1-51		WHT/BRN
-52	A5J1-52		WHT/RED
J7-53	A5J1-53	GND	WHT/ORN

Table G-4. Motherboard Wire List (Core Memory Processor)-Continued

FROM	TO	FUNCTION	COLOR
J7-54	A5J1-54		WHT/YEL
J7-55	CHASSIS	CHASSIS GND	BLK
J8-1	A6J1-1	GND	BRN
-2	A6J1-2		RED
J8-3	A6J1-3		ORN
J8-4	A6J1-4		YEL
-5	A6J1-5		GRN
-6	A6J1-6		BLU
-7	A6J1-7		VIO
-8	A6J1-8		GRA
-9	A6J1-9		WHT
-10	A6J1-10		BLK
-11	A6J1-11		WHT/BRN
-12	A6J1-12		WHT/RED
-13	A6J1-13	GND	WHT/ORN
-14	A6J1-14		WHT/YEL
-15	A6J1-15		WHT/GRN
-16	A6J1-16		WHT/BLU
-17	A6J1-17		WHT/VIO
-18	A6J1-18		WHT/GRA
-19	A6J1-19		WHT
-20	A6J1-20		BLK
-21	A6J1-21		BRN
-22	A6J1-22		RED
-23	A6J1-23		ORN
-24	A6J1-24		YEL
-25	A6J1-25		GRN
-26	A6J1-26		BLU
-27	A6J1-27		VIO
-28	A6J1-28		GRA
-29	A6J1-29		WHT
-30	A6J1-30		BLK
-31	A6J1-31		WHT/BRN
J8-32	A6J1-32		WHT/RED
J8-33	A6J1-33		WHT/ORN
-34	A6J1-34	GND	WHT/YEL
-35	A6J1-35		WHT/GRN
-36	A6J1-36		WHT/BLU
-37	A6J1-37		WHT/VIO
-38	A6J1-38		WHT/GRA
J8-39	A6J1-39		WHT

Table G-4. Motherboard Wire List (Core Memory Processor). Continued

FROM	TO	FUNCTION	COLOR
J8-40	A6J1-40		BLK
-41	A6J1-41		BRN
-42	A6J1-42		RED
-43	A6J1-43		ORN
-44	A6J1-44		YEL
-45	A6J1-45		GRN
-46	A6J1-46		BLU
-47	A6J1-47		VIO
-48	A6J1-48		GRA
-49	A6J1-49		WHT
-50	A6J1-50		BLK
-51	A6J1-51		WHT/BRN
-52	A6J1-52		WHT/RED
-53	A6J1-53	GND	WHT/ORN
-54	A6J1-54		WHT/YEL
J8-55	CHASSIS	CHASSIS GND	BLK
J9-1	A7J1-1	GND	BRN
-2	A7J1-2		RED
-3	A7J1-3		ORN
-4	A7J1-4		YEL
-5	A7J1-5		GRN
J9-6	A7J1-6		BLU
J9-7	A7J1-7		VIO
-8	A7J1-8		GRA
-9	A7J1-9		WHT
-10	A7J1-10		BLK
-11	A7J1-11		WHT/BRN
-12	A7J1-12		WHT/RED
-13	A7J1-13	GND	WHT/ORN
-14	A7J1-14		WHT/YEL
-15	A7J1-15		WHT/GRN
-16	A7J1-16		WHT/BLU
-17	A7J1-17		WHT/VIO
-18	A7J1-18		WHT/GRA
-19	A7J1-19		WHT
-20	A7J1-20		BLK
-21	A7J1-21		BRN
-22	A7J1-22		RED
-23	A7J1-23		ORN
-24	A7J1-24		YEL
J9-25	A7J1-25		GRN

Table G-4. Motherboard Wire List (Core Memory Processor)-Continued

FROM	TO	FUNCTION	COLOR
J9-26	A7J1-26		BLU
-27	A7J1-27		VIO
-28	A7J1-28		G RA
-29	A7J1-29		WHT
-30	A7J1-30		BLK
-31	A7J1-31		WHT/BRN
-32	A7J1-32		WHT/RED
-33	A7J1-33		WHT/ORN
-34	A7J1-34	GND	WHT/YEL
J9-35	A7J1-35		WHT/GRN
J9-36	A7J1-36		WHT/BLU
-37	A7J1-37		WHT/VIO
-38	A7J1-38		WHT/GRA
-39	A7J1-39		WHT
-40	A7J1-40		BLK
-41	A7J1-41		BRN
-42	A7J1-42		RED
-43	A7J1-43		ORN
-44	A7J1-44		YEL
-45	A7J1-45		GRN
-46	A7J1-46		BLU
-47	A7J1-47		VIO
-48	A7J1-48		GRA
-49	A7J1-49		WHT
-50	A7J1-50		BLK
-51	A7J1-51		WHT/BRN
-52	A7J1-52		WHT/RED
-53	A7J1-53	GND	WHT/ORN
-54	A7J1-54		WHT/YEL
J9-55	CHASSIS	CHASSIS GND	BLK
J10-1	A8J1-1	GND	BRN
-2	A8J1-2		RED
-3	A8J1-3		ORN
-4	A8J1-4		YEL
-5	A8J1-5		GRN
-6	A8J1-6		BLU
-7	A8J1-7		VIO
-8	A8J1-8		GRA
J10-9	A8J1-9		WHT
J10-10	A8J1-10		BLK
J10-11	A8J1-11		WHT/BRN

Table G-4. Motherboard Wire List (Core Memory Processor)-Continued

FROM	TO	FUNCTION	COLOR
10-12	A8J1-12	GND	WHT/RED
-13	A8J1-13		WHT/ORN
-14	A8J1-14		WHT/YEL
-15	A8J1-15		WHT/GRN
-16	A8J1-16		WHT/BLU
-17	A8J1-17		WHT/VIO
-18	A8J1-18		WHT/GRA
-19	A8J1-19		WHT
-20	A8J1-20		BLK
-21	A8J1-21		BRN
-22	A8J1-22		RED
-23	A8J1-23		ORN
-24	A8J1-24		YEL
-25	A8J1-25		GRN
-26	A8J1-26		BLU
-27	A8J1-27		VIO
-28	A8J1-28		GRA
-29	A8J1-29		WHT
-30	A8J1-30		BLK
-31	A8J1-31		WHT/BRN
-32	A8J1-32		WHT/RED
-33	A8J1-33		WHT/ORN
-34	A8J1-34	GND	WHT/YEL
-35	A8J1-35		WHT/GRN
-36	A8J1-36		WHT/BLU
-37	A8J1-37		WHT/VIO
J 10-38	A8J1-38		WHT/GRA
J 10-39	A8J1-39		WHT
-40	A8J1-40		BLK
-41	A8J1-41		BRN
-42	A8J1-42		RED
-43	A8J1-43		ORN
-44	A8J1-44		YEL
-45	A8J1-45		GRN
-46	A8J1-46		BLU
-47	A8J1-47		VIO
-48	A8J1-48		GRA
-49	A8J1-49		WHT
-50	A8J1-50		BLK
-51	A8J1-51		WHT/BRN
J10-52	A8J1-52		WHT/RED

Table G-4. Motherboard Wire List (Core Memory Processor)-Continued

FROM	TO	FUNCTION	COLOR
J 10-53	A8J1-53		WHT/ORN
-54	A8J1-54		WHT/YEL
J 10-55	CHASSIS	CHASSIS GND	BLK

Table G-5. AC Power Supply Assembly Model 5617 Wire List

FROM	TO	FUNCTION	COLOR
A4 P15-A2	E703	+ 5V RTN	BLACK
A4P15-A3	E703	+ 5V RTN	BLACK
A4P15-A4	E702	+ 5V	WHITE
A4 P15-A5	E702	+ 5V	WHITE

Table G-6. DC Power Supply Assembly Model 5687 Wire List

FROM	TO	FUNCTION	COLOR
A3 E303	E703	+5 SENSE RTN	ORN
A3 E302	E702	+5 SENSE	RED
A4 P15-A2	E703	+ 5V RTN	BLK
A4 P15-A3	E703	+ 5V RTN	BLK
A4 P15-A4	E702	+ 5V	WHT
A4 P15-A5	E702	+ 5V	WHT
A3T300-FL1	E701		
A3T300-FL2	CR700		
A3T300-FL3	CR700		
A3T300-FL4	CR701		
A3T300-FL5	CR701		
E704	E700	+ 5V	WHT
E705	E700	+ 5V	WHT

Table G-7. AC Power Unit Assembly Wire List

FROM	TO	FUNCTION	COLOR
P1-4	TB1-2	AC PHASE A	BLK
-5	TB1-3	AC PHASE B	RED
P1-6	TB1-4	AC PHASE C	WHT
SHIELD	CHAS GND		
E1	TB1-1		WHT
E2	TB1-3		WHT
B1-1	TB1-1	FAN	BLU
B1-2	TB1-2	FAN	RED
B1-3	TB1-3	FAN	YEL
SHIELD	CHAS GND		
B1-1	TB1-1	FAN	GRN
B1-2	TB1-2	FAN	YEL
B1-3	TB1-3	FAN	RED
SHIELD	CHAS GND		
B1-1	TB1-1	FAN	YEL
B1-2	TB1-2	FAN	RED
B1-3	TB1-3	FAN	GRN
SHIELD	CHAS GND		
B1-1	TB1-2	FAN	RED
B1-2	TB1-3	FAN	YEL
B1-3	TB1-4	FAN	BLU
SHIELD	CHAS GND		

GLOSSARY

ALU	Arithmetic Logic Unit
AMDF	Army Master Data File
apex	Appendix
AIR	Air-Transport Rack
BITE	Built-In Test
CPU	Central Processing Unit
DISREP	Discrepancy in Shipment Report
DMA	Direct Memory Access
EIR	Equipoment improvement Recommendations
ERIC	Error Correction Code
ESML	Expendable Supplies & Materials List
ELM	Elapsed Time Meter
FLU	Floating Point Unit
lMC/RMC	Internal Memory Control/Remote Memory Control
I/O	Input/Output
MAC	Maintenance Allocation Chart
MEMIN	Memory In
MEMOUT	Memory Out
MTU	Magnetic Tape Unit
NSN	National Stock Numbers
PCB	Printed-Circuit Boards
PFP	Prefetch Professor

GLOSSARY —Continued

PMCS	Preventive Maintenance Checks and Services
PROM	Programmable Read Only Memory
PWR	Power
RAM	Random Access Memory
ROD	Report of Discrepancy
TAMMS	The Army Maintenance Management System
TMDE	Test, Measurement, and Diagnostic Equipment
UART	Universal Asynchronous Receiver/Transmitter
VC	Virtual Consol

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RECOMMENDED CHANGES TO EQUIPMENT TECHNICAL PUBLICATIONS

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10 July 1975

PUBLICATION NUMBER	PUBLICATION DATE	PUBLICATION TITLE
TM 11-5840-340-12	23 Jan 74	Radar Set AN/PRC-76

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PAGE NO	PARAGRAPH	FIGURE NO	TABLE NO
2-25	2-28		
3-10	3-3		3-1
5-6	5-8		
		F03	

IN THIS SPACE TELL WHAT IS WRONG AND WHAT SHOULD BE DONE ABOUT IT:

Recommend that the installation antenna alignment procedure be changed throughout to specify a 2^{o} IFF antenna lag rather than 1^{o}.

REASON: Experience has shown that with only a 1^{o} lag, the antenna servo system is too sensitive to wind gusting in excess of 25 knots, and has a tendency to rapidly accelerate and decelerate as it hunts, causing strain to the drive train. Hunting is minimized by adjusting the lag to 2^{o} without degradation of operation.

Item 5, Function column. Change "2 db" to "3db."

REASON: The adjustment procedure for the TRANS POWER FAULT indicator calls for a 3 db (500 watts) adjustment to light the TRANS POWER FAULT indicator.

Add new step f.1 to read, "Replace cover plate removed in step e.1, above."

REASON: To replace the cover plate.

Zone C 3. On J1-2, change "+24 VDC to "+5 VDC."

REASON: This is the output line of the 5 VDC power supply. +24 VDC is the input voltage.

PRINTED NAME, GRADE OR TITLE AND TELEPHONE NUMBER
SSG I. M. DeSpiritof 999-1776

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I. M. DeSpiritof

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